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(71) Applicant:
SEIKO EPSON CORPORATION
Tokyo 163 (JP)

(72) Inventor:
MATSUEDA, Yojiro,
Seiko Epson Corporation
Nagano-ken 392 (JP)

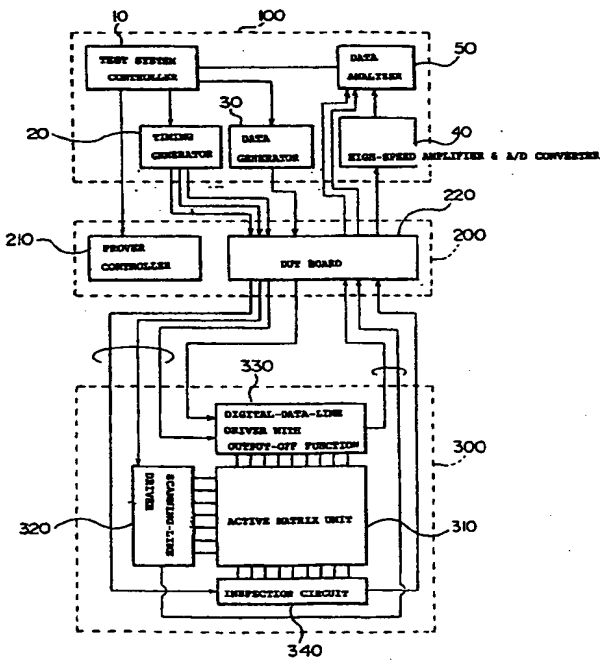
(74) Representative:
Sturt, Clifford Mark et al
Miller Sturt Kenyon
9 John Street
London WC1N 2ES (GB)

(54) METHOD FOR INSPECTING ACTIVE MATRIX BOARD, ACTIVE MATRIX BOARD, LIQUID CRYSTAL DEVICE AND ELECTRONIC EQUIPMENT

(57) A digital driver (330), having the function of enabling an output terminal to be in high-impedance condition, for driving data lines, and an inspection circuit (340) provided at ends of the data lines opposite to the digital driver are provided. The inspection circuit (340) includes bidirectional switches provided for each of the plurality of respective data lines, and control means for controlling the switching of the switches.

By using the inspection circuit provided at the opposite ends of the data lines, not only inspections of data-line disconnection or digital-driver output but also determination of whether or not there is a point defect can be performed. In addition, since the circuit is designed only for inspection, its size is extremely small, and the circuit can be disposed in a dead space.

FIG. 1



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Description

[Technical Field]

[0001] The present invention relates to an active-matrix- substrate inspecting method, an active matrix substrate, a liquid crystal device and an electronic apparatus, and in particular, to techniques for inspecting a type of active matrix substrate in which a digital data-line driver (driver in which a digital signal is input and converted from digital to analog form to output an analog signal for driving data lines) (hereinafter referred to as a "digital driver") is formed on the substrate.

[Background Art]

[0002] In recent years, researches have been actively made on an active matrix substrate with a built-in driver in which driving circuits (drivers) for scanning lines and data lines are formed on a substrate, and a liquid-crystal display device using the substrate. Such an active matrix substrate is produced using low-temperature polysilicon techniques, for example. In order to put the products in which the above substrate is used on the market, it is required to perform an inspection of conforming article/non-conforming articles accurately from a liliabiliry guarantee point of view after the substrate is formed but before a panel is assembled.

[0003] According to the study of the present inventor, the above-described inspection mainly requires basic inspections such as checking the drivers' output ability and detecting a disconnection of the data lines, and inspections of the characteristics of switching devices (TFTs, MIMs, etc.) included in pixels and the leak characteristics of storage capacitors, which relate to an inspection on a point defect in an active matrix unit.

[0004] In the case of a digital driver for driving the data lines (namely, digital-data-line driver), a method for performing simultaneous driving at predetermined timing (line-at-a-time driving method) has been employed as a result of paying attention to the ease of digital data storage.

[0005] A display device with such a built-in digital-line-at-a-time-driving driver has not been realized, so that how the above-described highly reliable inspections are performed is not clear.

[0006] Accordingly, one object of the present invention is to establish a technique for inspecting an active matrix substrate including a digital driver mounted thereon so that highly reliable substrates and display devices, etc. can be put on the market.

[Disclosure of Invention]

[0007] In order to solve the foregoing problems, the present invention has the following structures. The present invention includes: a plurality of scanning lines and a plurality of data lines;

a digital driver having the function of enabling an output terminal to be in high-impedance condition, said digital driver being provided for driving the plurality of data lines;

switching devices each connected to a respective scanning line and a respective data line;

capacitors connected to respective switching devices; and

an inspection circuit provided at ends of the data lines opposite to the digital driver, and

the inspection circuit includes respectivebi-directional switches provided for each of the plurality of data lines, and control means for controlling the switching of the switches.

[0008] Since the digital driver for the data lines has a D/A converter in an output unit, it cannot inspect an active matrix unit (measurement of point defects) by reading a once output signal again via a common channel.

[0009] However, according to the present invention, since the inspection circuit is provided at the opposite ends of the data lines to the digital driver, signals can be written in the capacitors (storage capacitors) in the active matrix unit by driving the data lines with the digital driver, and the written signals can be read out through the inspection circuit. Accordingly, determination of whether or not there is a point defect can be made.

[0010] In signal reading with the inspection circuit, when the output of the digital driver (A/D conversion output) is on, defect determination based on signals read out from the storage capacitors is not secured. Thus, in a step for acquiring a basic signal for point-defect determination, the output of the inspection circuit needs to be switched off (set to be high-impedance condition). Therefore, the digital driver includes the function of enabling the output to be in high-impedance condition.

[0011] In addition, since the inspection circuit is provided as a circuit used for inspection, it does not need to operate at high speed like as the digital driver, and it needs only a minimum function, for example, capable of performing inspection. Accordingly, according to the present invention, the digital driver has a structure including bi-directional switches (e.g., analog switches) and control means for controlling the switching of the switches. Its simplified circuit arrangement and no requirement of advanced operating characteristics need only a small transistor size, which is suitable for space reduction. Therefore, the inspection circuit can be mounted on the active matrix substrate, easily.

[0012] The "inspection circuit" means a circuit mainly used for inspection and not having the function of driving the data lines like as the digital driver, but does not exclude the use of another object different from inspection and the inclusion of a component usable for an object other than inspection.

[0013] Devices included in the inspection circuit may be produced, together with devices included in the dig-

ital driver, by an identical production process.

[0014] On one active matrix substrate, a digital driver and an inspection circuit are produced by an identical process. For example, using low-temperature polysilicon-thin-film-transistor (TFT) techniques enables the production.

[0015] The digital driver includes a switch in its output unit, and opening the switch causes the output unit to be in high-impedance condition.

[0016] The switch is provided in the output unit in order to make the output of the digital driver be in high-impedance condition.

[0017] The digital driver includes any one of a switched capacitor D/A converter, a resistor ladder D/A converter and a PWM D/A converter.

[0018] Examples of a D/A converter mountable on an active matrix substrate of the present invention are shown.

[0019] In a switched capacitor D/A converter, for example, switches are provided for each of the weighted capacitors, and the charge of each capacitor is combined with a coupling capacitor by control of the switching of the switches so as to generate a conversion voltage.

[0020] In a resistor ladder D/A converter, for example, a resistance-divided voltage is selectively extracted by control of the switching of the switches provided at the output channels so as to generate a conversion voltage.

[0021] In a PWM D/A converter, for example, the on-duration of a switch connected to a voltage source in which a voltage value varies with time (ramp-wave) is controlled in accordance with a digital data value so as to generate a conversion voltage.

[0022] The control means in the inspection circuit performs point-at-a-time scanning of the bi-directional switches.

[0023] The inspection circuit has, for example, a point-at-a-time scanning system of data lines using shift registers etc. and performs inspection by the point-at-a-time reading of data.

[0024] When the number of the bi-directional switches is M (where M is a natural number not less than 2), the control means in the inspection circuit repeatedly performs the simultaneous driving of P (where P is a natural number) bi-directional switches Q (where Q is a natural number) times, whereby the driving M ($M = P \times Q$) bidirectional switches in total is realized.

[0025] The inspection circuit uses a method different from point-at-a-time scanning.

[0026] At least a part of the inspection circuit is disposed in a space, which is in the active matrix substrate and not contributing to the realization of substantial functions, such as displaying an image.

[0027] Since the inspection circuit needs only a small transistor size and a small occupied area, at least a part of the inspection circuit can be disposed in a space, which is in the active matrix substrate and not contributing to the realization of substantial functions, such as displaying an image, namely, a so-called dead space. Therefore, the enlargement of the active matrix substrate and liquid-crystal display device can be suppressed.

[0028] The inspection circuit is disposed in a sealing position formed by sealing material in a panel production process.

[0029] The position to be sealed by the sealing material in a panel production process is a dead space inevitably generated in the active matrix substrate. By disposing the inspection circuit in this space, the effective use of space can be achieved.

[0030] Each of the inspection circuit and the digital driver is divided into plural pieces and disposed on the active matrix substrate.

[0031] There are the cases that disposing separated circuits enables a dead space to be used more effectively. By the amount of the separation, the number of devices in one block is reduced, and enough space for the layout is produced. In addition, by the amount of reducing the number of devices, the operating frequency of a shift register or the like which operate in series can be reduced.

[0032] The inspection circuit is separated into at least a first inspection circuit and a second inspection circuit, while the digital driver is separated into at least a first digital driver and a second digital driver,

the first digital driver and the first inspection circuit are disposed to be mutually opposed, with the data lines provided therebetween, and the second digital driver and the second inspection circuit are disposed to be mutually opposed, with the data lines provided therebetween, and

the first digital driver and the second inspection circuit are disposed at identical ends of the data lines, and the second digital driver and the first inspection circuit are disposed at identical ends of the data lines.

[0033] There is formed a layout in which the separated identical-type circuits (each of the first circuit and the second circuit) are disposed at the opposite sides of the data lines provided between them.

[0034] Since the circuits are dispersed and disposed on the top and bottom surfaces of the active matrix substrate, dead space around the display region is easy to effectively use. In particular, there are dead spaces, uniformly at sealing positions around (at the top and bottom of) the substrate, which is advantageous when the spaces are effectively used.

[0035] In addition, the circuit separation reduces the number of devices in one circuit block in accordance with the number of separations, which produce enough space for the layout. By the amount of reducing the number of devices, the operating frequency of a shift register or the like which operates in series can be reduced.

[0036] There is provided a method for inspecting an active matrix substrate, the method comprising the steps of:

writing signals in the capacitors connected to the switches by using the digital driver to drive the data lines;

causing the output of the digital driver to be in high-impedance condition; and

acquiring a basic signal to be a basis of inspection by reading the signals written in the capacitors by the inspection circuit, and inspecting an active matrix unit, based on the acquired signal.

[0037] Next, a basic method for inspecting an active matrix unit using an active matrix substrate is described as follows.

[0038] The inspection of the digital driver itself and the disconnection inspection of the data lines are performed before each step is executed.

[0039] Before the active matrix unit is inspected, the output characteristics of a digital driver itself and disconnection of data lines are inspected (preliminary inspection).

[0040] According to the above-described active matrix substrate of the present invention, an inspection circuit is disposed opposing to a digital driver, with data lines provided between them. Thus, the preliminary inspection can be easily performed based on the reception or the amplitude of the received signals and so on by the means that the line-at-a-time driving of each data line is performed, for example, once, by using the digital driver, then the inspection circuit is scanned by either line-at-a-time scanning or point-at-a-time scanning being synchronizing with the scanning of the data lines and the signals sent via the data lines are received.

[0041] The step of inspecting the active matrix unit, based on the acquired basic signals, includes the step of considering the two-dimensional distribution of the basic signal characteristics in the active matrix unit.

[0042] In many cases, the basic signal to be acquired for inspecting the active matrix unit includes considerable noise. Accordingly, it is effective to perform relative inspection with consideration on not only the absolute value of the signal characteristic but abnormality in the signal characteristic distribution (e.g., the existence of a particular portion indicating abnormality in the form of a significant point, compared with the neighborhood, and so on).

[0043] The step of inspecting the active matrix unit, based on the acquired basic signal, includes the step of comparing the acquired basic signal with a sample signal, which is previously prepared.

[0044] This is a method for inspection performed by comparison with a sample signal. The liquid crystal device is assembled with an active matrix substrate, and has high reliability having passed predetermined inspection. Further, the liquid crystal device comprises an active matrix substrate and has a high reliability having passed predetermined inspection. The electric apparatus including the liquid crystal device has also high reliability owing to the high reliability of the liquid cyrystal device.

[Brief Description of the Drawings]

[0045]

Fig. 1 is a block diagram showing an apparatus for executing one example of an active-matrix-substrate inspecting method of the present invention.

Fig. 2 is a block diagram showing an example of circuits mounted on an active matrix substrate of the present invention.

Fig. 3 is a chart showing the schematic comparison between the size of a transistor included in the D/A converter in Fig. 2 and the size of a transistor included in the inspection circuit in Fig. 2

Fig. 4 is a sectional view of a main part of a liquid-crystal display device, showing an example in which the inspection circuit is disposed below a sealing material.

Fig. 5 is a flowchart showing an outline of one embodiment of an active-matrix-substrate inspecting method of the present invention.

Fig. 6 is a flowchart illustrating more specific details of the active-matrix-substrate inspecting method of an embodiment of the present invention.

Fig. 7 is a flowchart showing more specific details of the point defect measurement in Fig. 6.

Fig. 8 is a flowchart showing more specific details of the status determination in Fig. 6.

Fig. 9 consists of (a) a plan view showing one example of the structure of one pixel included in an active matrix unit, and (b) an equivalent circuit diagram of the structure in (a).

Fig. 10 consists of (a) a plan view showing another example of the structure of one pixel included in the active matrix unit, and (b) an equivalent circuit diagram of the structure in (a).

Fig. 11 is a chart illustrating an outline of a structural example of a capacitance-divisional D/A converter usable in the present invention.

Fig. 12 is a diagram showing an structural example of the circuit of a part of the capacitance-divisional D/A converter in Fig. 11.

Fig. 13 is a diagram illustrating an outline of a structural example of a resistance-divisional D/A converter usable in the present invention.

Fig. 14 is a diagram illustrating an outline of a structural example of a PWM D/A converter usable in the present invention.

Fig. 15 consists of (a) and (b) diagrams illustrating an outline of one example of the inspection circuits shown in Fig. 1 and Fig. 2, respectively.

Fig. 16 is a diagram illustrating an outline of another example of the structure of the inspection circuits shown in Fig. 1 and Fig. 2.

Fig. 17 is a diagram showing another example of a structure of the circuits mounted on the active

matrix substrate of the present invention.

Fig. 18 is a chart showing positions used when a glass substrate is cut in order to produce an active matrix substrate.

Fig. 19 is a chart showing a layout of a scanning-line driving circuit, a data-line scanning circuit, an inspection circuit, and so on.

Fig. 20 is a chart showing a first step in an embodiment of an active-matrix-substrate producing method of the present invention.

Fig. 21 is a chart showing a second step in the embodiment of the active-matrix-substrate producing method of the present invention.

Fig. 22 is a chart showing a third step in the embodiment of the active-matrix-substrate producing method of the present invention.

Fig. 23 is a chart showing a fourth step in the embodiment of the active-matrix-substrate producing method of the present invention.

Fig. 24 is a chart showing a fifth step in the embodiment of the active-matrix-substrate producing method of the present invention.

Fig. 25 is a chart showing a sixth step in the embodiment of the active-matrix-substrate producing method of the present invention.

Fig. 26 is a chart showing a seventh step in the embodiment of the active-matrix-substrate producing method of the present invention.

Fig. 27 is a chart showing the structure of a liquid-crystal display device in which an active matrix substrate of the present invention is used.

Fig. 28 is a chart showing one example (laptop computer) of an electronic apparatus in which an active matrix substrate of the present invention is used.

Fig. 29 is a chart showing another example (liquid-crystal projector) of the electronic apparatus in which an active matrix substrate of the present invention is used.

Fig. 30 consists of (a) a sectional structure view of the device taken on line A-A shown in Fig. 9(a), and (b) a sectional structure view of the device taken on line A-A shown in Fig. 10(a).

[0046] In the drawings, the reference numerals denote the following.

10 test system controller
20 timing generator
30 data generator
40 high-speed amplifier and A/D converter
100 active-matrix-substrate tester
200 full-autoprover
210 prover controller
220 DUT board
300 active matrix substrate
310 active matrix unit
320 scanning liner driver
330 digital-data-line driver with an output-off function
340 inspection circuit

[Best Mode for Carrying Out the Invention]

[0047] A more detailed description will be given with reference to the following embodiments of the present invention which are shown in the drawings.

(First Embodiment)

(1) Outline of an Inspection System and its Operation

[0048] Fig. 1 is a block diagram showing a whole composition of an apparatus for executing one example of an active-matrix-substrate inspecting method of the present invention.

[0049] This embodiment describes a case where an active matrix substrate (hereinafter referred to as a "TFT substrate") having switching devices, in a pixel portion, composed of thin film transistors (TFTs), is inspected.

[0050] In Fig. 1, a TFT substrate tester 100 includes a test system controller 10 for monitoring and controlling an inspection operation, a timing generator 20 for generating various timing signals, a data generator 30 for outputting data for inspection, a high-speed amplifier and A/D converter 40, and a data analyzer 50 to which data output from the A/D converter is input and which performs predetermined analysis.

[0051] The full-autoprover 200 includes a prover controller 210 and a DUT board 220 as an interface of various signals.

[0052] A TFT substrate 300 has an active matrix unit, a scanning line driver 320, a digital-data-line driver 330 with an output-off function (hereinafter simply referred to as a "digital-data-line driver"), and an inspection circuit 340. The output-off function is the function of enabling output to forcedly be in high impedance condition. In inspection, a probe (an inspection, terminal not shown in Fig. 1) of the full-autoprover is connected to a predetermined terminal (not shown in Fig. 1) in which the TFT substrate 300 is exposed.

[0053] In addition, under the monitoring and control of the test system controller 10, timing signals and inspection data are output from the timing generator 20 and the data generator 30 in the TFT substrate tester 100. These are sent to the TFT substrate 300 via the DUT board 220 in the full-autoprover 200.

[0054] The timing signals are input to the scanning-line driver 320 in the TFT substrate 300, the digital-data-line driver 330, and the inspection circuit 340, respectively, and the inspection data are input to the digital-data-line driver 330.

[0055] After a predetermined inspection process ends (details of inspection operation will be described below), the inspection circuit 340 outputs an acquired analog

signal (hereinafter referred to as a "basic signal"), which is a basis for inspection, and this basic signal is sent to the TFT tester 100 via the DUT board 220 in the full-autoprover 200. It is amplified and converted from analog to digital form by the high-speed amplifier and A/D converter in the TFT tester 10, and the converted data are input to the data analyzer 50, in which the predetermined analysis of them is performed.

(2) Outline of Circuits Formed on the TFT Substrate 300

[0056] In Fig. 2, an example of a specific block diagram of the TFT substrate 300 shown in Fig. 1 is shown. In order to enable an inspection using the inspection system shown in Fig. 1 to be performed, the TFT substrate 300 needs to fulfill several necessary conditions.

[0057] In other words, the necessary conditions are that the digital-data-line driver has an output-off function (the function of enabling output to be in high impedance condition) and that each pixel portion has a capacitance in substrate condition.

[0058] As shown in Fig. 2, the digital-data-line driver 330, built into the TFT substrate 300, includes an m-bit shift register 400, a in-bit-data input terminal (D1 to Du, u x m switches SW1 to SWum, a u x m-bit latch A (reference numeral 410) and a latch B (reference numeral 420)), and an m-bit D/A converter 430. In this embodiment, the D/A converter 430 has an output-off function.

[0059] The scanning line driver 320 includes an n-bit shift register 322.

[0060] The active matrix unit includes a plurality of data lines X1 to Xm, a plurality of scanning lines Y1 to Yn, TFTs (M1), which are arranged in a matrix and are connected to respective scanning lines and the data lines, and storage capacitors (holding capacitors) C_{S1}. The existence of the storage capacitors C_{S1} enables point defects in substrate condition to be measured.

[0061] In TFT substrate condition, no liquid crystal capacitors C_{LC} exist. However, in Fig. 2, in consideration of the ease of understanding, the liquid crystal capacitors C_{LC} are shown for convenience. In addition, terminals of the storage capacitors C_{S1}, opposite to their terminals to the TFTs (M1), are held to have a common potential V_{COM}.

(3) Specific Structures

1. Structure of Storage Capacitor

[0062] In Fig. 9, (a) and (b), the structure of one pixel in the active matrix unit in Fig. 2 is shown.

[0063] In Fig. 9, (a) shows its layout, and (b) shows its equivalent circuit. The sectional structure of the device taken on line A-A in Fig. 9(a) is shown in Fig. 30 (a).

[0064] In Fig. 9 (a), reference numerals 5000, 5100 denote scanning lines, and reference numerals 5200, 5300 denote data lines. In addition, reference numeral 5400 denotes a capacitor line, and reference numeral 5500 denotes a pixel electrode.

[0065] As is clear from Fig. 30(a), an insulating film 5520 similar to an insulating film 5510 is formed between an extension 5505 of the drain of a TFT, and a capacitor line 5400 simultaneously formed using a step for forming a scanning line (gate electrode) 5000, and an interlayer insulating film 5530 is formed between the capacitor line 5400 and the pixel electrode 5500. These constitute a storage capacitor (C_{S1}) 5410. Reference numeral 5600 denotes an aperture (region through which light is transmitted), and K1, K2 denote contact regions.

[0066] The storage capacitor (C_{S1}) can be formed using the structure as shown in Fig. 10, (a) and (b). In Fig. 30(b), the sectional structure of the device taken on line A-A in Fig. 10(a) is shown.

[0067] In Fig. 9, the capacitor lines are separately formed. However, in Fig. 10, the storage capacitor is formed by causing the extension of the TFT drain to overlap with an adjacent scanning line (gate electrode).

[0068] In other words, as shown in Fig. 10(a) and Fig. 30(b), an insulating film 5130 similar to a gate insulating film 5120 is formed between a drain extension 5700 consisting of polysilicon, and an adjacent scanning line (gate electrode) 5100, and an interlayer insulating film 5140 is formed between the adjacent scanning line 5100 and the pixel electrode 5500. These constitute a storage capacitor 5420. In Fig. 10(a), portions corresponding to those in Fig. 9(a) are denoted by identical reference numerals.

② Structure of D/A Converter

[0069] Those having structures shown in Fig. 11 to Fig. 14 can be utilized to the m-bit D/A converter 430 in Fig. 2.

[0070] When a point defect inspection is performed, it is required that the output of a D/A converter is switched off after a signal is written in the capacitor of a pixel before. Accordingly, any of the D/A converters in Fig. 11 to Fig. 14 has an output-off function (the function of causing the output to be in high impedance condition). A specific description will be given below.

Switched capacitor D/A Converter

[0071] The D/A converter 430 in Fig. 11 is a switched capacitor D/A converter with an output-off function. In this converter, electric charge is accumulated in weighted capacitors (binary weight capacitors) C1 to C8, and when 8-bit input data D1 to D8 are "1", the corresponding switches (SW20 to SW28) are closed to transfer the electric charge between the respective capacitors (C1 to C8) and a coupling capacitor C30, whereby a conversion voltage corresponding to the 8-bit input data D1 to D8 is generated at an output terminal V_{OUT}. In Fig. 11, the switches (SW1 to SW8) are reset switches for the capacitors C1 to C8, and V0 is a reset

voltage. A switch C40 is a reset switch for the coupling capacitor C30.

[0072] A switch control circuit 6000 is provided in order to forcedly open the switches SW20 to SW28 so that the output terminal V_{OUT} is in floating condition (high impedance condition).

[0073] In Fig. 12, the specific structure of the switch SW20 is shown. The switch SW20 includes a transfer gate composed of an n-MOS transistor M10, a p-MOS transistor M20 and an inverter INV1, and an n-MOS transistor M30 connected in series to the transfer gate. The switch control circuit 6000 causes the output corresponding to the input data D1 to be in high impedance condition by switching off the n-MOS transistor M30. The other switches corresponding to the other input data can similarly be set in high impedance condition.

[0074] In Fig. 11 and Fig. 12, the switch control circuit 6000 is independently provided, and in Fig. 12, the special transistor (M30) for generating high impedance condition is provided. However, the arrangement is not always limited to these. For example, in Fig. 11 and Fig. 12, by using a reset signal or the like to forcedly fix the input data D1 to D8 to "0", the switch (SW20) in Fig. 11 and the transfer gates (M10, M20) in Fig. 12 can be switched off to set the output in high impedance condition.

Resistor ladder D/A Converter

[0075] The D/A converter 430 shown in Fig. 13 obtains a conversion output V_{OUT} by controlling the opening and closing of switches SW100 to SW108 to select and extract a divided voltage obtained from each of the common connection points of resistors R1 to R8 connected in series.

[0076] The opening and closing of the switches SW100 to SW108 is determined by the output of a decoder 7000. The switches SW100 to SW108 (switch group 7100) are controlled by a switch control circuit 7200 to be simultaneously opened, and the output can be set in high impedance condition.

PWN D/A Converter

[0077] The D/A converter 430 in Fig. 14 uses a PWM circuit 7502 to generate a pulse signal having a pulse width corresponding to the value of input data, and obtains a conversion output V_{OUT} by using the pulse width to control the on-duration (closed condition duration) of a switch 7506. Reference numeral 7504 denotes a ramp-wave power supply, and reference numeral 7400 denotes a latch circuit in which image data are temporarily stored. In addition, the control by the switch control circuit 7508 enables the switch 7506 to be forcedly opened, and the output to be in high impedance condition.

③ Structure of Inspection Circuit

[0078] Those drawn in Fig. 15, (a) and (b), and Fig. 16 are usable as the inspection circuit 340 shown in Fig. 2. The "inspection circuit" means that it is used for inspection and but is not used intending to drive the data lines like as the data line driver, but it does not exclude to have a structure to be used for a purpose other than inspection or or to use the whole circuit for a purpose other than inspection.

[0079] In the inspection circuit 342 in Fig. 15(a), MOS transistor-used analog switches SW_{X1} to SW_{xm} are provided corresponding to each of data lines X1 to Xm, and the point-at-a-time scanning of the analog switches SW_{X1} to SW_{xm} is performed with outputs from a shift register 7600, whereby basic signals to be a basis of the inspection can be obtained successively from an output terminal T_{OUT}. The basic signals are sent to the DUT board 220 in the full-autoprover 200.

[0080] In Fig. 15(b), one output from the shift register 7602 drives analog switches pairs (SW_{X1} to SW_{xm}), which is basically similar to that in Fig. 15(a) in the respect that point-at-a-time scanning is employed. By simultaneously driving two analog switches, the number of bits (the number of stages) only needs m/2 bits. In addition, the basic signals are obtained from two terminals T_{OUT1} and T_{OUT2}.

[0081] In the inspection circuit 342 in Fig. 16, a technique different from point-at-a-time scanning is employed. In other words, the technique is that, when m analog switches SW_{X1} to SW_{xm} are driven, p analog switches are simultaneously driven and the driving is repeatedly performed q times, whereby the driving of a total of m ($m = p \times q$) analog switches is realized.

[0082] A switch control circuit 7300 successively switches on control lines G1 to Gq, and whenever each control line is switched on, basic signals are simultaneously obtained from output lines L1 to Lp.

[0083] Since any of the above-described inspection circuits does not need a data-line driving ability, and has no requirement of high-speed driving for image display, its transistor size is allowed to be small, and it basically requires only a minimum operable ability. Accordingly, its occupied area can be extremely reduced, and it can be formed on a TFT substrate.

[0084] Fig. 3 shows the comparison between the size of a MOS transistor at the output stage of the D/A converter 430 on the condition that the D/A converter can perform point-at-a-time driving, and the size of a MOS transistor constituting the inspection circuit 342.

[0085] In other words, the channel width (W) of the MOS transistor M200 constituting the D/A converter 430, which is capable of point-at-a-time driving, needs at least 1000 μm or more. Conversely, the channel width (W) of the MOS transistor M300 constituting the inspection circuit 342 is preferably 100 μm or less. In other words, the size, which is necessary for the inspection-circuit transistor is 1/10 or less.

[0086] As described above, since the small transistor size and the reduced occupied area are allowed, it is possible to dispose at least a part of the inspection circuit 342 in space of the TFT substrate which does not contribute to realize substantial functions such as image display, in other words, so-called dead space. Therefore, the enlargement of the TFT substrate and the liquid-crystal display device can be suppressed.

[0087] For example, as shown in Fig. 4, the inspection circuit 342 can be disposed in a sealing position formed by the sealing material in a TFT-substrate panel Production process. In Fig. 4, for easy understanding, the sectional structure of a completed liquid-crystal display device is drawn.

[0088] In Fig. 4, reference numeral 500 denotes a glass substrate, reference numeral 510 denotes an SiO_2 film, reference numeral 520 denotes a gate-insulating film, reference numerals 530, 540 denote interlayer insulating films, reference numerals 522, 524 denote source-drain layers, and reference numeral 526 denotes a gate electrode.

[0089] The MOS transistor M300 constituting the inspection circuit is disposed in a sealing region A1 formed by a sealing material 550. The sealing position formed by the sealing material is a dead space inevitably generated in the active matrix substrate. By disposing the inspection circuit in this space, the space can effectively be used.

[0090] In Fig. 4, reference numeral 560 denotes a opposite substrate, reference numeral 570, 572 denote alignment layers, and reference numeral 574 denotes liquid crystal.

(4) Process for Inspecting a TFT Substrate

1. Outline

[0091] A TFT-substrate inspection is broadly divided into a step (preliminary inspection step, step 600 - Fig.5) for detecting disconnections of signal lines and inspecting an output from a D/A converter, and a step (step 610) for inspecting point defects.

[0092] The inspection (step 600) for detecting disconnections of signal lines and inspecting an output from a D/A converter is an inspection, which is realized by the basic structure of the active matrix substrate (Fig. 1, Fig. 2) of this embodiment. In the inspection, the inspection can performed, in general, by one scanning by switching on all the outputs of the digital-data-line driver 330 and using the inspection circuit 340 to receive the outputs.

[0093] For example, in case that no output signals from the data line driver are transmitted via the data lines, it is determined that the data lines are disconnected, or the data line drive itself has a defect. The step (step 610) for inspecting point defects will be described below.

2. Specific Inspection Process

[0094] In Fig. 6, an example of a specific inspection process will be shown.

[0095] As to the flowchart in Fig. 6, a method in which inspection is performed in order of the required time for inspection, namely, an object requiring a short inspection time is inspected firstly, is employed, and according to this method, all necessary steps are inspected. However, the inspection process is not limited thereto, and in case that a defect is found, it is possible to stop performing the successive inspections. The inspection process in Fig. 6 will be in order described below.

[0096] At first, determination of whether there is or not a TFT substrate, which have not been inspected, is made. (step 700). If there is a TFT substrate, which have not been inspected, the substrate is aligned to (mounted on) the system in Fig. 1 (step 700), and then the proving with the full-autoprover 220 in Fig. 1 is performed (step 720).

[0097] In addition, a driver-consumed current is measured (step 730). This step determines whether a consuming current flowing in the data lines and a power supply for the scanning driver (and the inspection circuit) is in a normal range or not. In case that short-circuiting occurs in the power supply, an excess current flows, then the determination can be performed.

[0098] Next, an end pulse of the scanning line driver is measured (step 740). In other words, a pulse is input in the first stage of the shift register, and determination of whether the pulse is output from the final stage at predetermined timing is performed. Since the pulse is a digital signal, instant determination can be performed.

[0099] Next, an end pulse of the data line driver is measured similarly to the case of the scanning line driver (step 750).

[0100] Next, short-circuit inspection of the data lines (signal lines) and the scanning lines is executed (step 760).

[0101] In other words, a current flowing from the scanning line driver to the inspection circuit is measured with all the outputs of the scanning driver set to high level, and each switch in the inspection circuit switched on,. If short-circuiting occurs in the interconnection, an excess current flows.

[0102] Next, disconnection inspection of the data lines (signal line) and the scanning lines is executed (step 770).

[0103] In other words, with all the outputs of the digital driver set to high level, a current change is detected by successively closing the switches of the inspection circuit. If there is a disconnection, the flowing current decreases, which enables the detection.

[0104] Next, the outputs of the D/A converter are measured (step 780).

[0105] Before point-defect inspection is performed, all the outputs of the D/A converter are inspected. In this inspection, in order to enhance its precision, it is prefer-

able to check whether the output levels of signals having a plurality of gray scale: white, black and intermediate tone, are proper or not.

[0106] Specifically, a voltage set at a predetermined level is output to all the data lines (signal lines), then the output of the D/A converter is set to have high impedance condition after a given time, and the voltage of each inspection circuit (signal line) is detected using the inspection circuit.

[0107] Next, point-defect measurement is performed (step 790).

[0108] More specifically, this point-defect measurement is performed according to the process shown in Fig. 7. In other words, signals are written in the storage capacitors in the pixels (step 900) by switching on all out put of the digital data line driver so that the voltage set at a predetermined level is output to all the data lines (signal lines). Next, the outputs of the D/A converters of the digital-data-line driver are set to be a high impedance condition (step 910). Next, a fluctuation of potential for each pixel is detected(step 920) by selecting the scanning lines one by one with the switches are closed. In addition, if necessary, a plurality of detections (step 930) and the detections with different writing conditions (step 940) are executed.

[0109] If an abnormality (defect) is found in any of each of the above steps, the defect address is detected if needed, and it is used as basic data for status determination (step 800 in Fig. 6).

[0110] Since the basic data to be a basis for the detection are obtained in the above steps, comprehensive status determination is performed based on the basic data (step 810 in Fig. 6).

[0111] For example, the status determination is comprehensively performed such that, as shown in Fig. 8, the two-dimensional distribution of the basic data on the TFT substrate is considered to find whether or not a portion (significant point) showing a numerical value extremely different from that of the neighborhood (step 960), and an abnormality is searched by using sample data for comparison.(step 970).

[0112] In addition, the above inspection steps are performed in order for other chips, which have not been inspected (steps 820, 830 in Fig. 6).

[0113] As described above, according to this embodiment, conforming-article inspection of an active matrix substrate with a built-in digital data-line driver can precisely be performed in short time.

(Second Embodiment)

[0114] A second embodiment of the present invention will be described using Fig. 17.

[0115] A feature of this embodiment is that digital-data-line drivers and inspection circuits is disposed being divided into upward and downward, and the upward and downward separate circuits are disposed well closely each other to realize a compact structure.

[0116] As shown in Fig. 17, the digital-data-line drivers are composed of the two: a first driver 8000A and a second driver 8000B. The structure of digital-data-line driver itself is identical to that in Fig. 2. However, the two-parts division causes the number of bits of each driver is 1/2 of that in Fig. 2.

[0117] In addition, the inspection circuits are composed of the two: a first circuit 8100A and a second circuit 8100B. The first circuit 8100A is connected to even data lines (X2, X4 to Xm), and the second circuit 8100B is connected to odd data lines (X1, X3 to Xm-1). In Fig. 17, reference numerals S1, S2, S3, S4, Sm and Sm-1 denote analog switches, and reference numerals 8102 and 8104 denote one-stage shift registers.

[0118] By dividing drivers and inspection circuits as described in this embodiment, various advantages, described below, can be obtained.

[0119] In other words, dividing drivers and inspection circuits enables the number of devices constituting each circuit to be half, the occupied area to be reduced that much , and the arrangement of the devices to be performed with clearance.

[0120] In addition, halving the number of shift-register stages also halves the operating frequency, which is advantageous in circuit design.

[0121] Moreover, circuit division leads to the uniform arrangement of circuits disposed around pixels, which enables the efficient use of a dead space. For example, this is advantageous to utilize the dead space right under the sealing material, described in Fig. 4.

[0122] In other words, the sealing material is provided so that its uniform width touches the periphery of the substrate, without exerting an excess stress on the substrate. Accordingly, the divided circuits and the reduced number of circuit devices are useful in enhancing the efficiency of using the dead space right under the sealing material.

[0123] In particular, the device size of inspection-circuits is smaller than the driver device size. Thus, dividing the inspection circuit reduces the space, which is advantageous in layout design.

[0124] In Fig. 19, an example of the arrangement of an inspection circuit etc. on an active matrix substrate (TFT substrate) is shown. Fig. 19 shows not only the layout of drivers etc. on the active matrix substrate but also vertically sectional and transversely sectional surfaces of a liquid crystal panel including the TFT substrate.

[0125] In Fig. 19, reference numeral 9100 denotes an active matrix substrate (TFT substrate), reference numerals 8000A and 8000B denote a digital-data-line driver and an inspection circuit, and reference numeral 320 denotes a scanning line driver. In addition, reference numeral 8300 denotes a light-shielding pattern, in which there is an active matrix unit (pixels). Reference numeral 8400 denotes a mounting terminal unit, reference numeral 9200 denotes a sealing material, reference numeral 574 denotes liquid crystal, and reference numeral 9000 denotes a opposite substrate opposite

substrate (color filter-formed substrate).

[0126] As is clear from Fig. 19, any of the scanning line driver, the data line driver and the inspection circuit is disposed effectively utilizing the dead spaces around the active matrix substrate. Accordingly, this arrangement is adapted to effectively use the dead space in the sealing position by the sealing material.

[0127] The liquid crystal panel (active matrix substrate 9100) shown in Fig. 19 is produced through a cutting step, for example, as shown in Fig. 18.

[0128] In other words, in Fig. 18, an active matrix substrate (TFT substrate) 9100 and a opposite substrate (color-filter substrate) 9000 are adhered to each other by a large-size adhering technique, and then they are cut to produce six panels. In Fig. 18, cutting lines (L10, L11, L30, L31, L32, L33) indicated by alternate long and short dash lines are lines at which the active matrix substrate and the opposite substrate are simultaneously cut. Cutting lines (L20, L21) indicated by dotted lines are lines at which only the opposite substrate is cut.

(Third Embodiment)

[0129] In this embodiment, a method (production method using low-temperature polysilicon techniques) for producing thin film transistors (TFT) on an active matrix substrate will be described using Fig. 20 to Fig. 26.

[0130] In the process in Fig. 20 to Fig. 26, capacitors (condenser) are also produced. Accordingly, this process can be used for not only the production of an inspection circuit and a shift registers of a driver but the production of the switched capacitor D/A converter in Fig. 11.

Step 1

[0131] Initially, as shown in Fig. 20, a buffer layer 4100 is formed on a substrate 4000, and an amorphous silicon layer 4200 is formed on the buffer layer 4100.

Step 2

[0132] Next, as shown in Fig. 21, annealing is performed by emitting a laser beam to the whole surface of the amorphous silicon layer 4200. As a result, the amorphous silicon is polycrystalized to form a polycrystal silicon layer 4220.

Step 3

[0133] Next, as shown in Fig. 22, island regions 4230, 4240 and 4250 is formed by the patterning of the polycrystal silicon layer 4220 is performed.. The island regions 4230, 4240 and 4250 are layers in which the active regions (source, drain) of a MOS transistor are formed. In addition, the island region 4250 is a layer to be one electrode of a thin film capacitor.

Step 4

[0134] Next, as shown in Fig. 23, a mask layer 4300 is formed, and phosphorus (P) ions are doped into only the island region 4250 so that it has a low resistance.

Step 5

[0135] Next, as shown in Fig. 24, a gate-insulating film 4400 is formed, and TaN layers 4500, 4510 and 4520 are formed on the gate-insulating film. The TaN layers 4500 and 4510 are layers to be MOS transistor gates, and the TaN layer 4520 is a layer to be another electrode of a thin film capacitor. Subsequently, a mask layer 4600 is formed, and phosphorus (P) ions are doped by self-align to form a source layer 4231 and a drain layer 4232 which are an n-type, with the gate TaN layer 4500 as a mask.

Step 6

[0136] Next, as shown in Fig. 25, mask layers 4700a and 4700b are formed, and boron (B) ions are doped by self-align to form a source layer 4241 and a drain layer 4242 which are a p-type, with the gate TaN layer as a mask.

Step 7

[0137] Subsequently, as shown in Fig. 26, an interlayer insulating film 4800 is formed and contact holes are formed in the interlayer insulating film before electrode layers 4900, 4910, 4920 and 4930 composed of ITO and Al are formed. The electrodes are connected to the TaN layers 4500, 4510 and 4520, and the polycrystal silicon layer 4250, as well, via the contact holes, though, which are not shown in Fig. 26. This completes an n-channel TFT, a p-channel TFT and a MOS capacitor.

[0138] By using the above-described production process having common steps, production can be facilitated, which is advantageous also in cost. Further, since polysilicon has a carrier mobility extremely greater than amorphous silicon, high-speed operation is practical, which is advantageous in increasing circuit-operating speed.

[0139] In addition, since conforming-article determination is performed using the above-described inspection method, the reliability of finished products can extremely be increased. As a result, , high-quality products can be put into the market.

[0140] Although the above-described production process uses low-temperature polysilicon TFT techniques, the production method is not always limited to this. For example, if predetermined circuit-operating speed is guaranteed, a process using amorphous silicon can be used. In addition to TFTs, two-terminal devices such as MIMs can be used as switching devices in pixels.

(Fourth Embodiment)

[0141] In this embodiment, a liquid crystal panel produced using an active matrix substrate of the present invention, and an electronic device including said panel etc. will be described by way of example. Any of these is a high-quality apparatus.

1. Liquid-crystal Display Device (Fig. 27)

[0142] A liquid-crystal display device comprises a backlight 2000, a polarizer 2200, a TFT substrate 2300, liquid crystal 2400, a opposite substrate (color-filter substrate) 2500, and a polarizer 2600, for example as shown in Fig. 27. In this embodiment, as described above, a driving circuit 2310 (and an inspection circuit) is (/are) formed on a TFT substrate 2300.

2. Personal Computer (Fig. 28)

[0143] Personal computer 1200 shown in Fig. 28 has a main unit provided with a keyboard 1202, and a liquid-crystal display screen 1206.

3. Liquid-crystal Projector (Fig. 29)

[0144] Liquid-crystal projector 1100 shown in Fig. 29 is a projection-type projector with a transmissive liquid-crystal panel as a light bulb, and uses, for example, a three-plate-prism-method optical system.

[0145] In Fig. 29, in the projector 1100, projection light emitted from a white-light-source lamp unit 1102 is separated by a plurality of mirrors 1106 and two dichroic mirrors 1108 in a light guide 1104 into three primary colors RGB, and each of them is guided to three liquid-crystal panels 1110R, 1110G and 1110B for displaying respective color images. The rays modulated by the respective liquid-crystal panels 1110R, 1110G and 1110B are incident on the dichroic prism 1112 from three directions. In the dichroic prism 1112, the red R and blue B rays are bent at 90°, and the green G ray travels straight. Thus, the respective color images are combined, and a color image is projected onto a screen etc. through a projection lens 1114.

[0146] In addition, electronic apparatuses to which the present invention can be applied include an engineering workstation (EWS), a pager or a portable telephone, a word processor, a television, a view-finder or monitor-direct-view video-cassette recorder, an electronic pocketbook, an electronic desk calculator, a car-navigation system, a POS terminal, an apparatus with a touch panel, and so on.

[Industrial Applicability]

[0147] The present invention relates to an active-matrix-substrate inspecting method, an active matrix substrate, a liquid crystal device, and an electronic apparatus, and in particular, to techniques for inspecting a type of active matrix substrate in which a digital type digital data-line driver (driver in which a digital signal is input and converted from digital to analog form to output an analog signal for driving data lines: hereinafter referred to as a "digital driver") is formed on the substrate.

Claims

1. An active matrix substrate including:

   a plurality of scanning lines and a plurality of data lines;
   a digital driver having the function of enabling an output terminal to be in high-impedance condition, said digital driver provided for driving the plurality of data lines;
   switching devices each connected to a respective scanning line and a respective data line;
   capacitors connected to respective switching devices; and
   an inspection circuit provided at ends of said data lines opposite to said digital driver,
   wherein said inspection circuit includes respective bidirectional switches provided for each of the plurality of data lines, and control means for controlling the switching of said switches.

2. An active matrix substrate according to Claim 1, wherein devices included in said inspection circuit are produced, together with devices included in said digital driver, by the same production process.

3. An active matrix substrate according to Claim 1 or Claim 2, wherein said digital driver has a switch in the output unit thereof, and said switch enables the output terminal to be in high-impedance condition when the switch is opened.

4. An active matrix substrate according to any one of Claim 1 to Claim 3, wherein said digital driver includes any one of a switched capacitor D/A converter, a resistor ladder D/A converter and a PWM D/A converter.

5. An active matrix substrate according to any one of Claim 1 to Claim 4, wherein said control means in said inspection circuit performs the point-at-a-time scanning of said bidirectional switches.

6. An active matrix substrate according to any one of Claim 1 to Claim 4, wherein, when the number of said bidirectional switches is M (where M is a natural number not less than 2), said control means in said inspection circuit repeatedly performs the simultaneous driving of P (where P is a natural

number) bidirectional switches Q (where Q is a natural number) times, thereby driving M (M = P × Q) bidirectional switches in total.

7. An active matrix substrate according to any one of Claim 1 to Claim 6, wherein at least a part of said inspection circuit is disposed in a space , which is in the active matrix substrate but does not contribute to realize substantial functions, such as displaying an image.

8. An active matrix substrate according to Claim 7, wherein said inspection circuit is disposed in a sealing position formed by sealing material in a panel production process.

9. An active matrix substrate according to any one of Claim 1 to Claim 8, wherein each of said inspection circuit and said digital driver is divided into plural pieces and disposed on said active matrix substrate.

10. An active matrix substrate according to Claim 9, wherein said inspection circuit is separated into at least a first inspection circuit and a second inspection circuit, while said digital driver is separated into at least a first digital driver and a second digital driver,

said first digital driver and said first inspection circuit are disposed with said data lines provided therebetween, and said second digital driver and said second inspection circuit are disposed with said data lines provided therebetween, and

said first digital driver and said second inspection circuit are disposed at identical ends of said data lines, and said second digital driver and said first inspection circuit are disposed at identical ends of said data lines.

11. A method for inspecting an active matrix substrate as set forth in any one of Claim 1 to Claim 10, said method comprising the steps of:

writing signals in said capacitors connected to said switches by using said digital driver to drive said data lines;
causing the output of said digital driver to be in high-impedance condition; and
acquiring a basic signal to be a basis of inspection by reading said signals written in said capacitors by said inspection circuit, and inspecting an active matrix unit, based on the acquired signal.

12. A method for inspecting an active matrix substrate, according to Claim 11, wherein the inspection of output function of said digital driver and the disconnection inspection of said data lines are performed before each step set forth in Claim 11 is executed.

13. A method for inspecting an active matrix substrate, according to Claim 11, wherein the step of inspecting the active matrix unit, based on the acquired basic signal includes the step of considering the two-dimensional distribution of the basic signal characteristics in said active matrix unit.

14. A method for inspecting an active matrix substrate, according to Claim 11, wherein the step of inspecting the active matrix unit, based on the acquired basic signal includes the step of comparing the acquired basic signal with a prepared sample signal.

15. A liquid crystal device including an active matrix substrate as set forth in any one of Claim 1 to Claim 10.

16. An electronic apparatus including a liquid crystal device as set forth in Claim 15.

FIG. 1

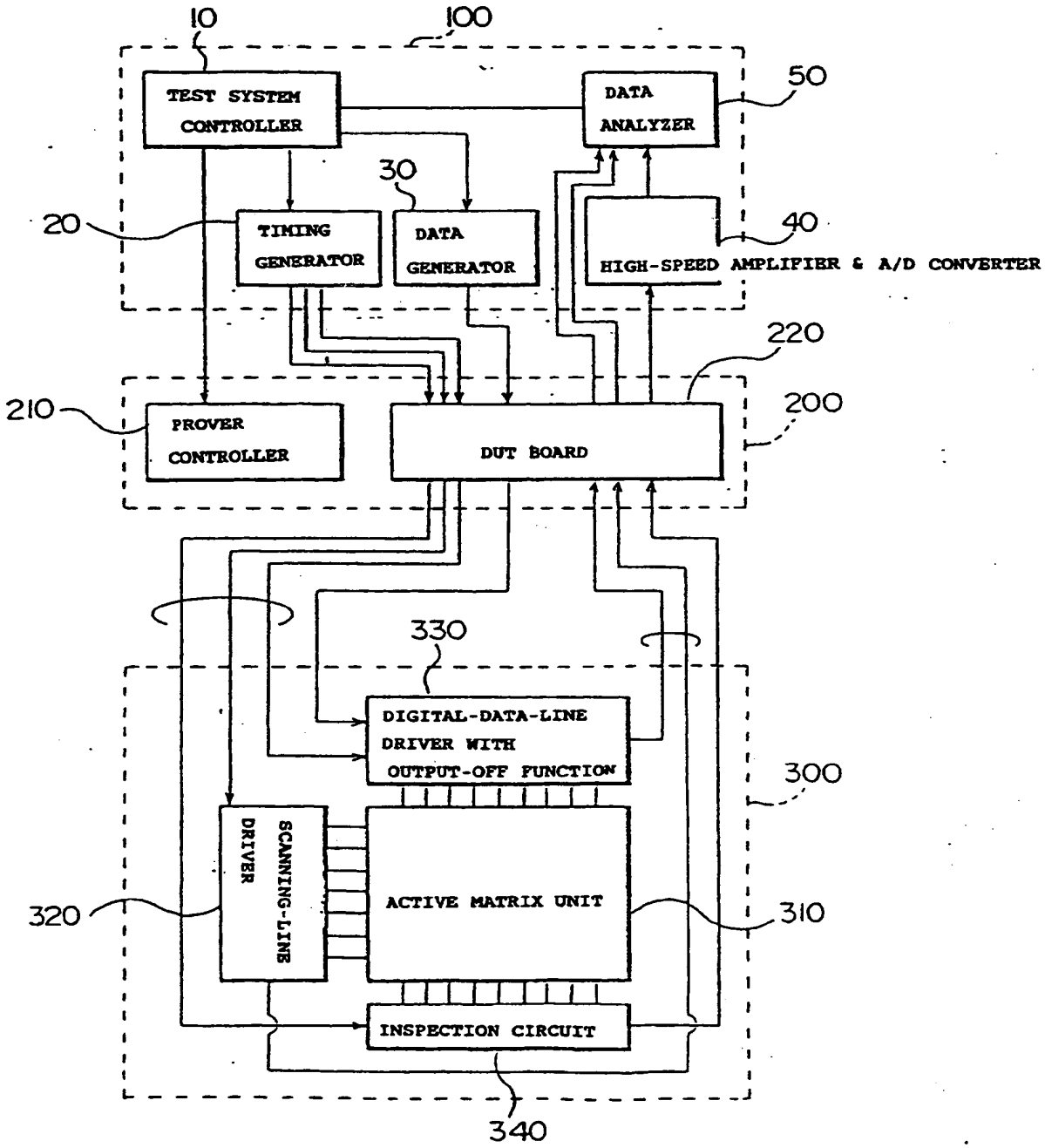


FIG. 2

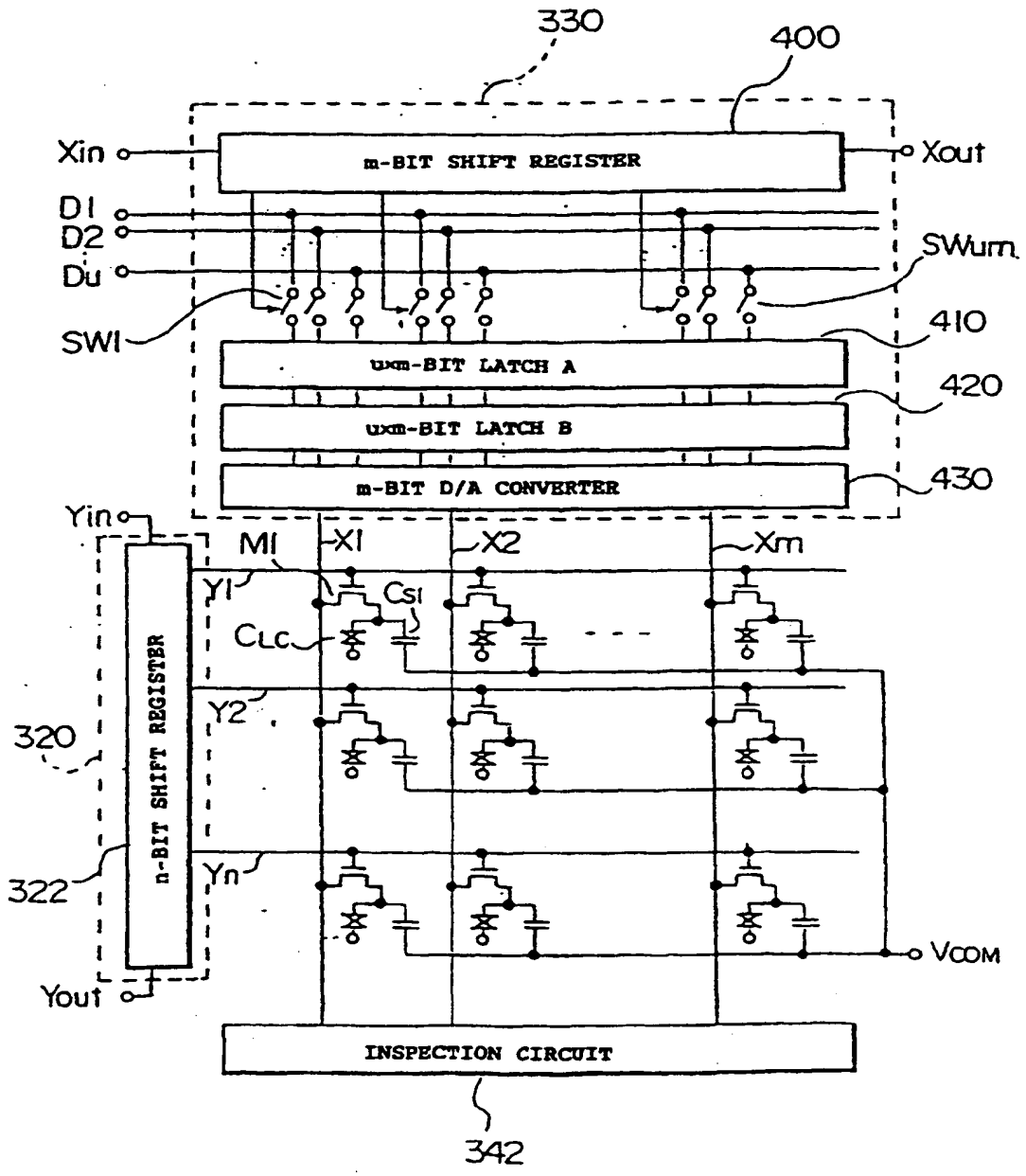


FIG. 3

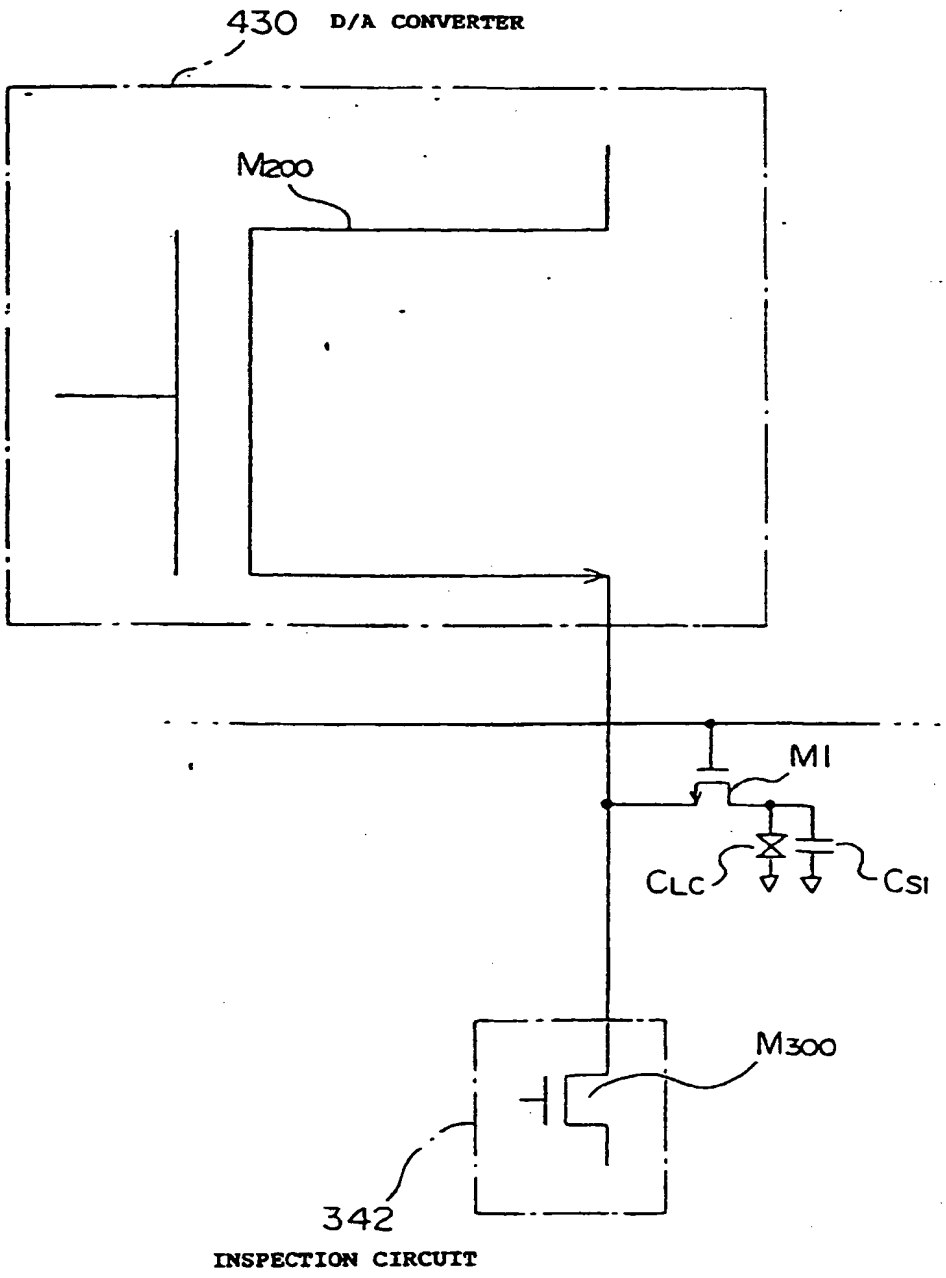


FIG. 4

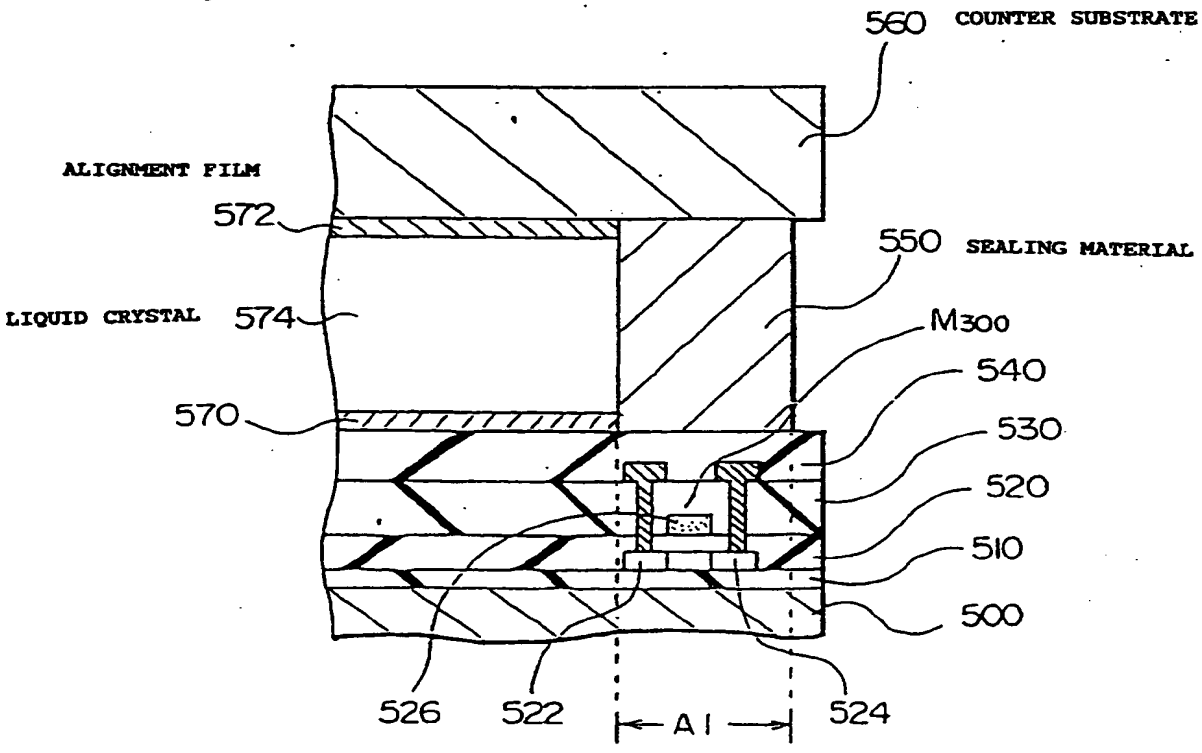


FIG. 5

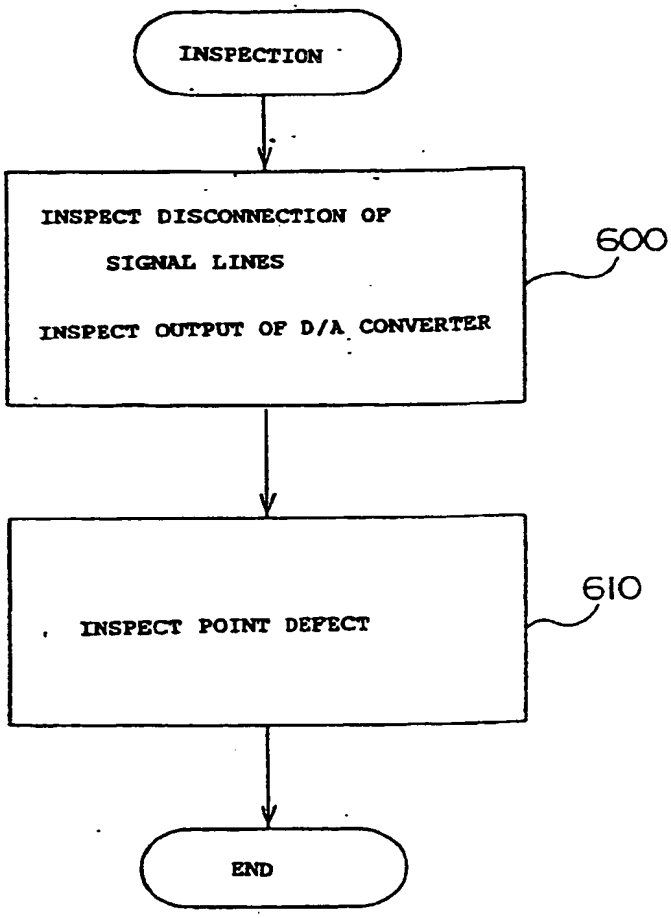


FIG. 6

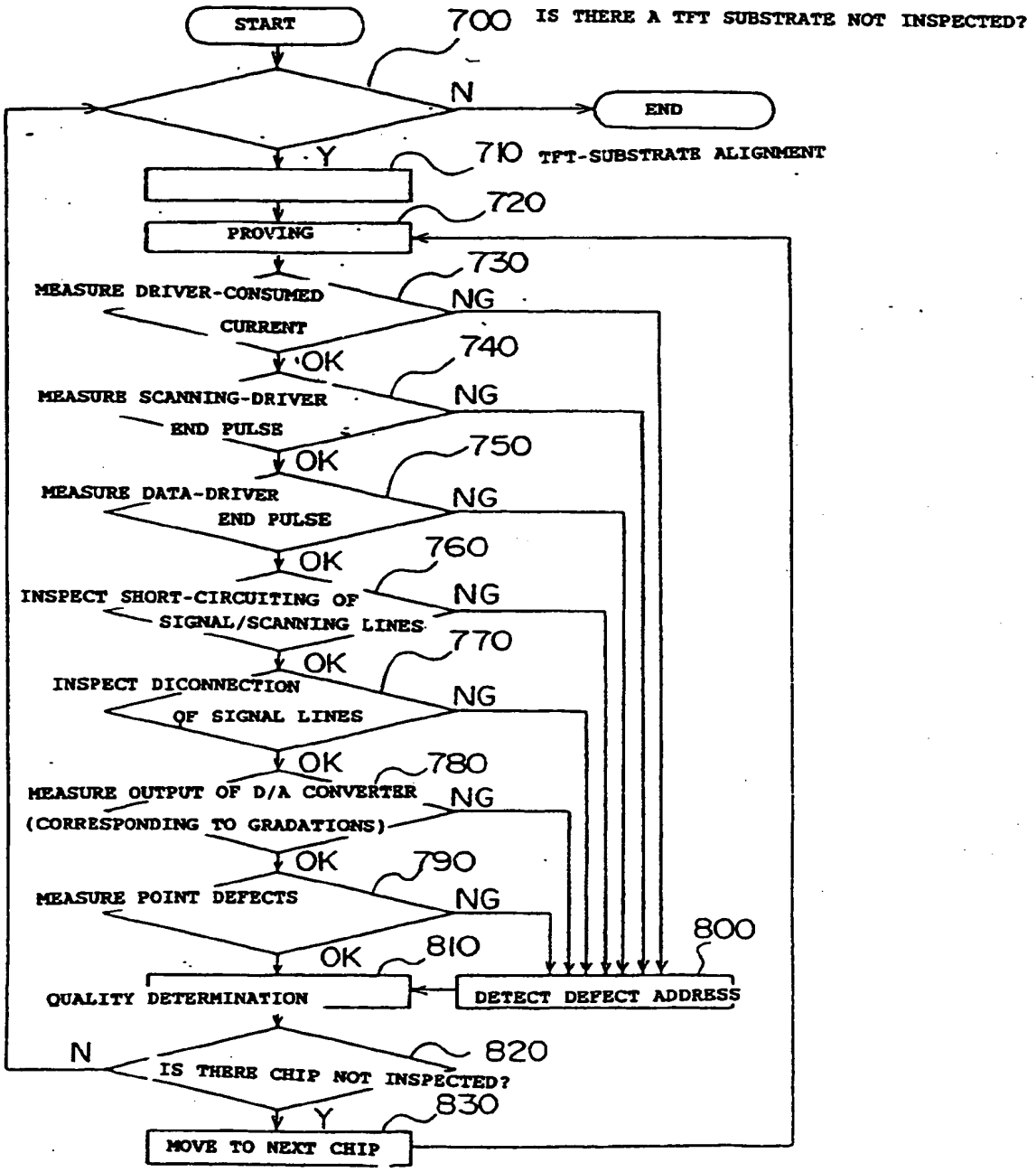


FIG. 7

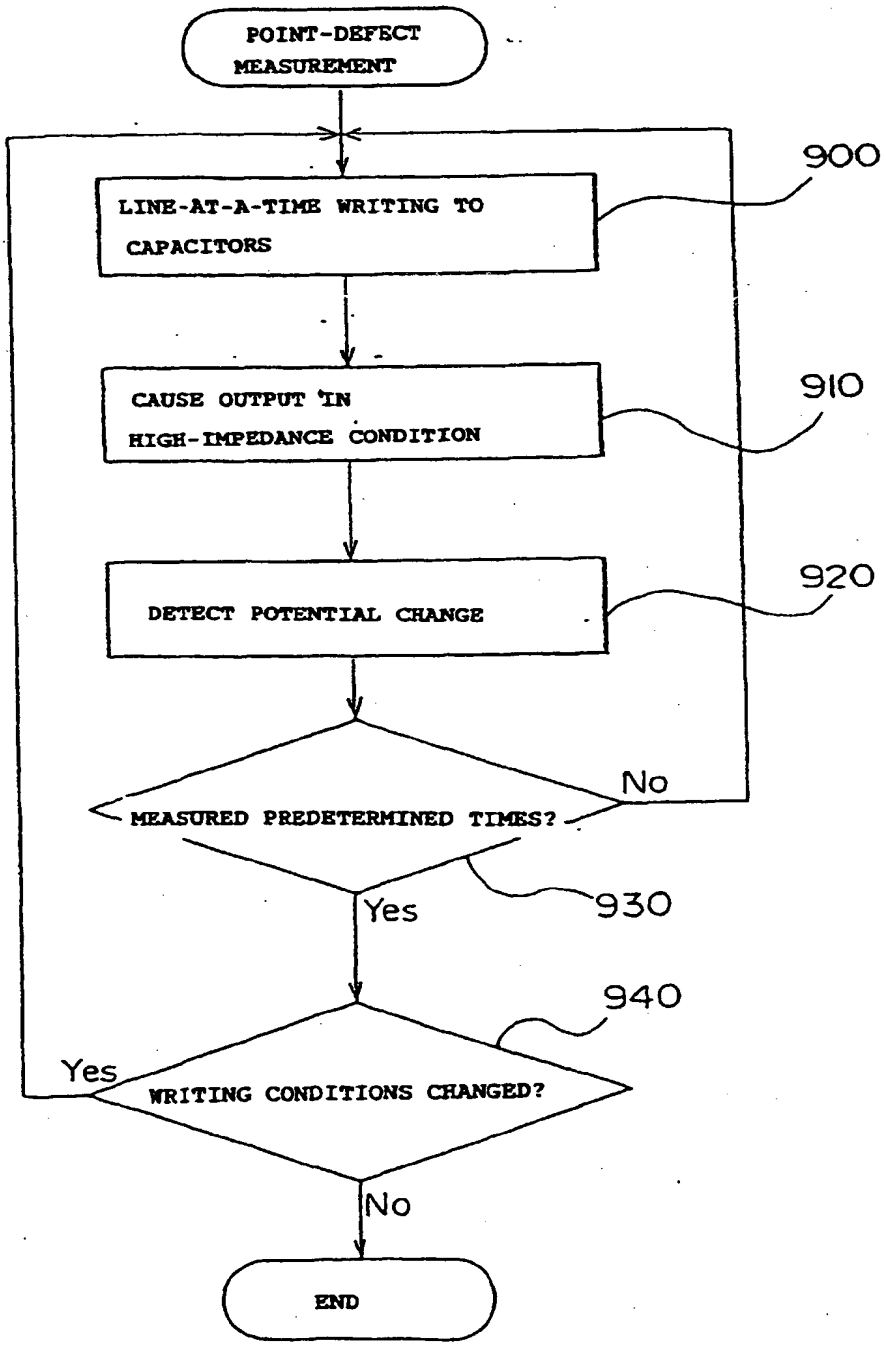


FIG. 8

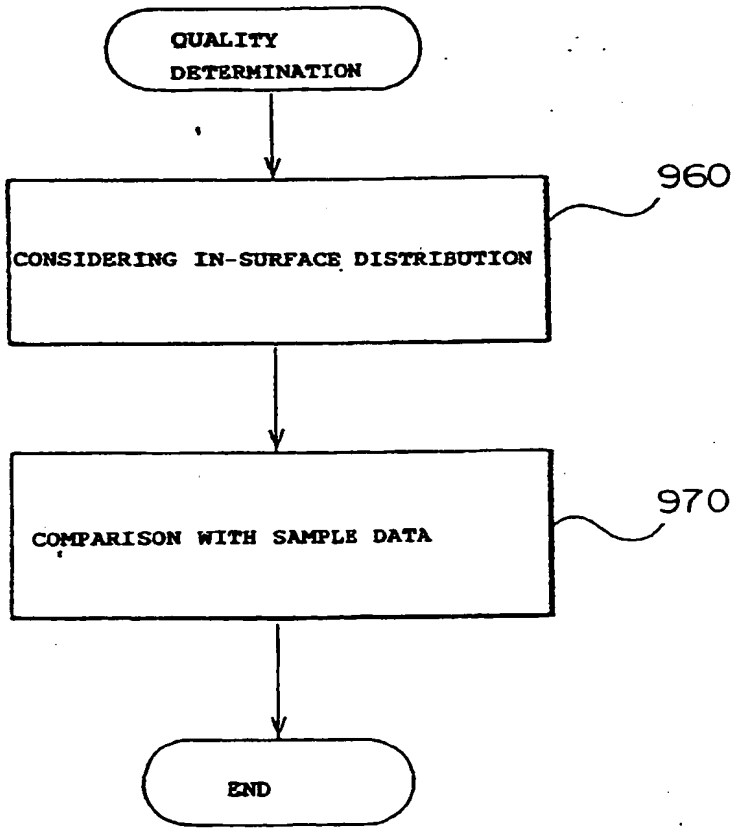

QUALITY DETERMINATION
960
CONSIDERING IN-SURFACE DISTRIBUTION
970
COMPARISON WITH SAMPLE DATA
END

FIG. 9

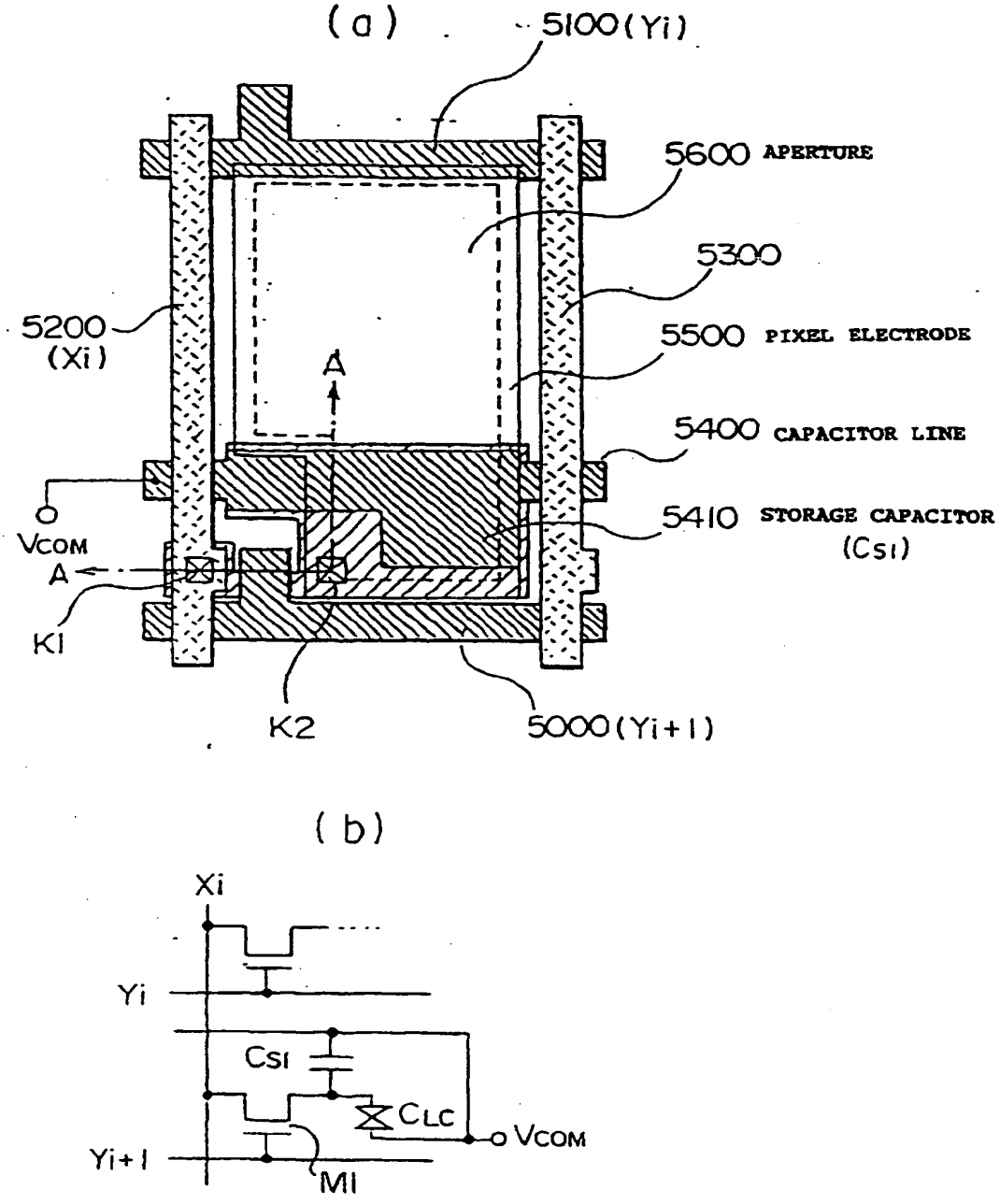


FIG. 10

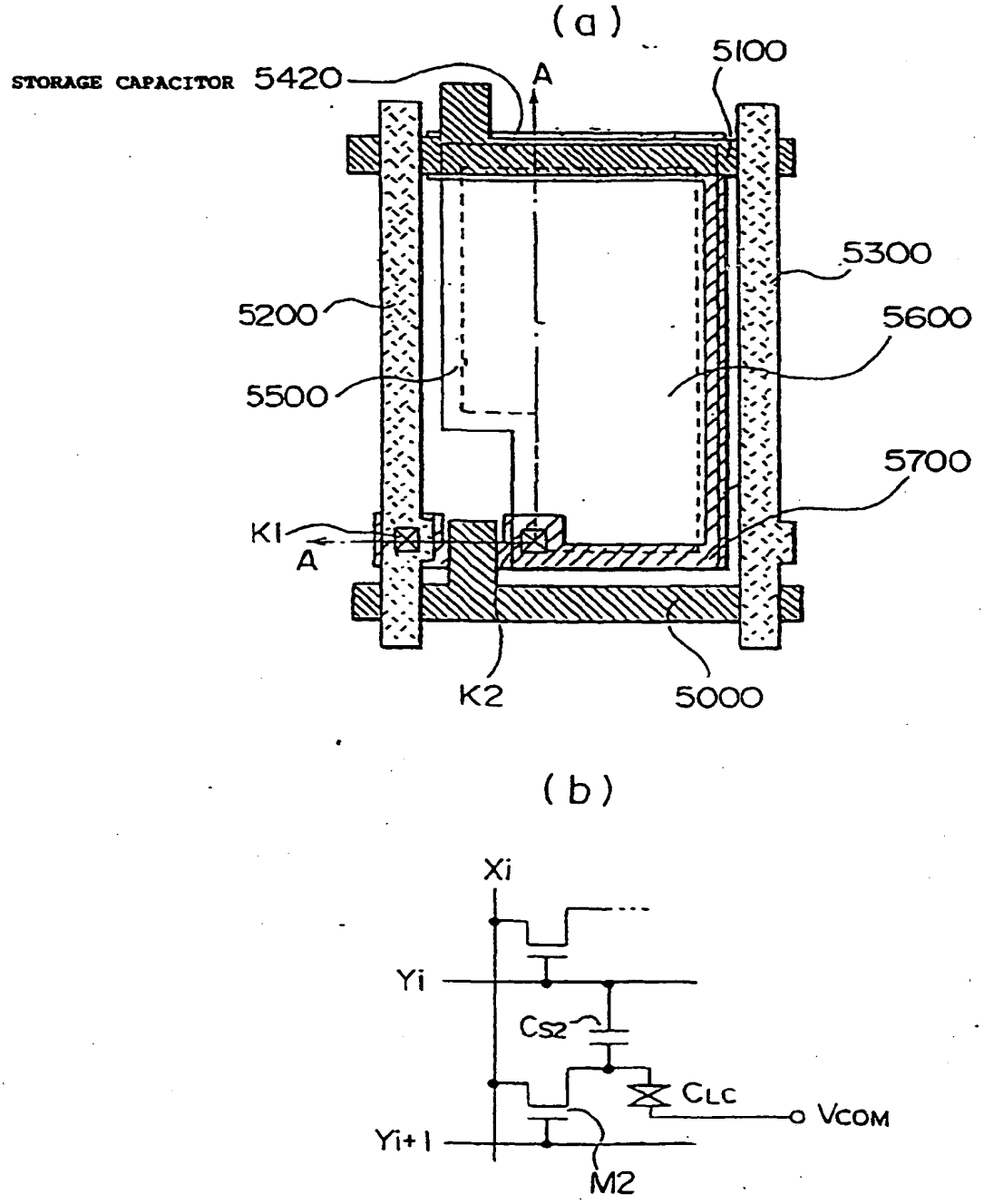

(a)
STORAGE CAPACITOR
5420
A
5100
5300
5200
5600
5500
5700
K1
A
K2
5000
(b)
Xi
Yi
Cs2
CLC
VCOM
Yi+1
M2

FIG. 11

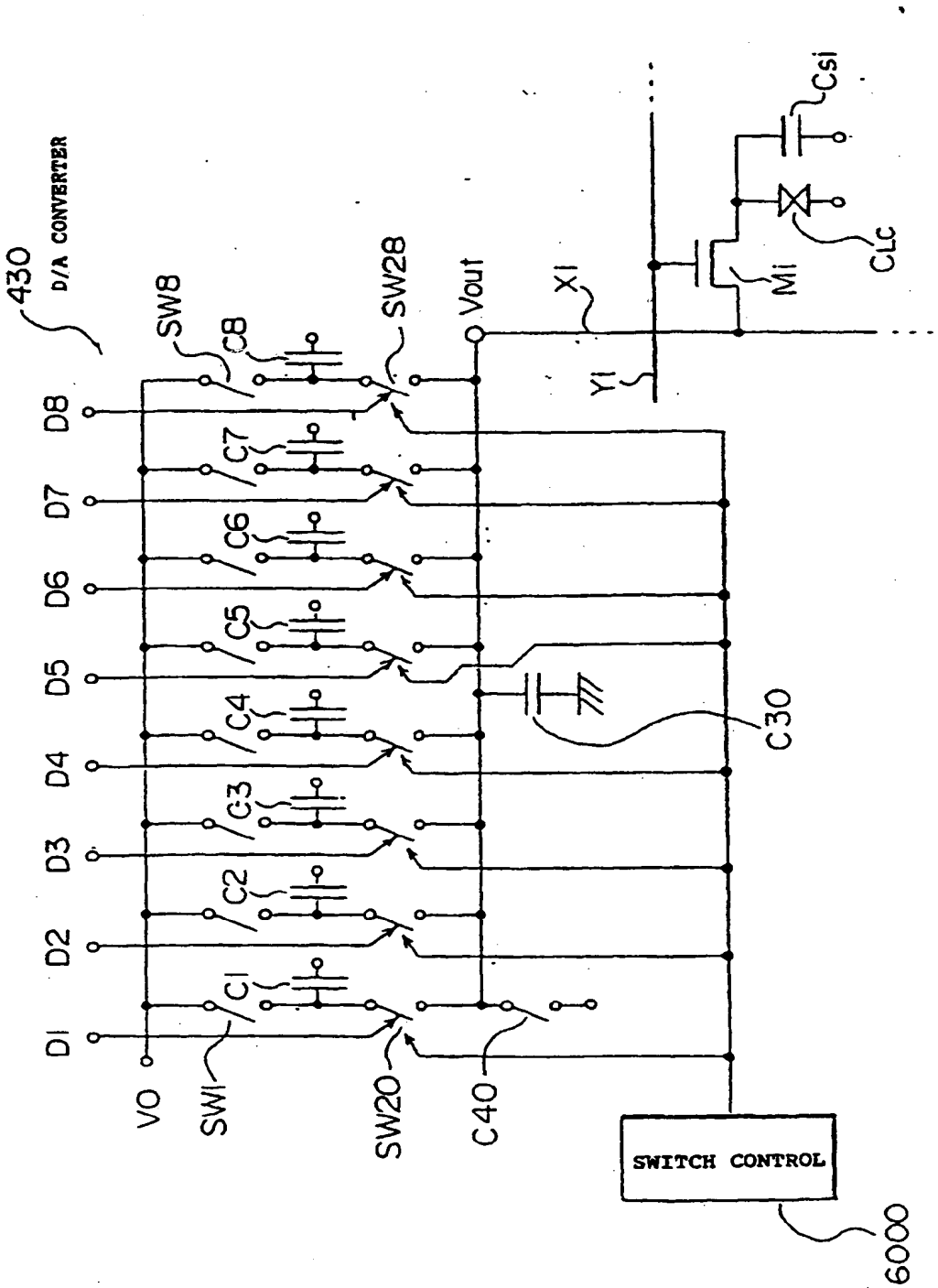


FIG. 12

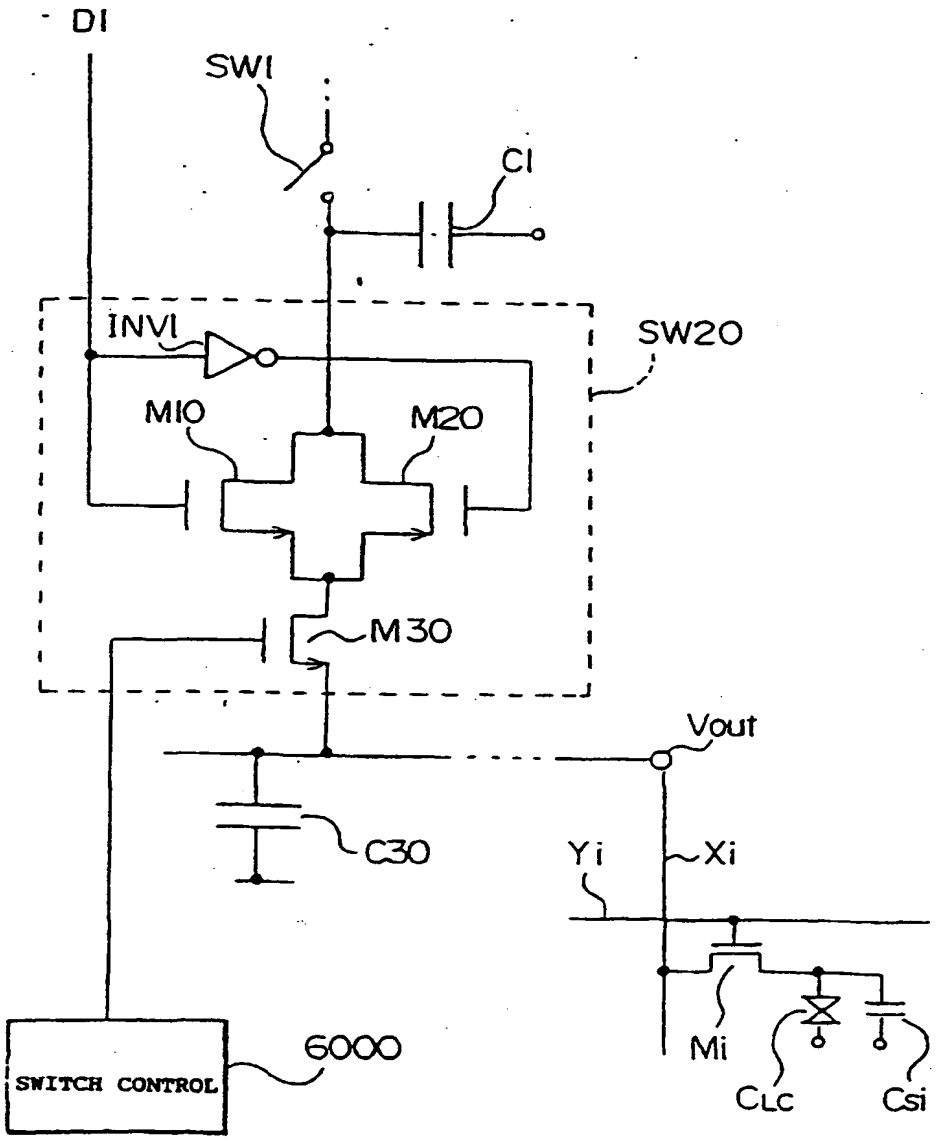

DI
SWI
CI
INVI
SW20
MIO
M20
M30
Vout
C30
Yi
Xi
Mi
CLC
Csi
SWITCH CONTROL
6000

FIG. 13

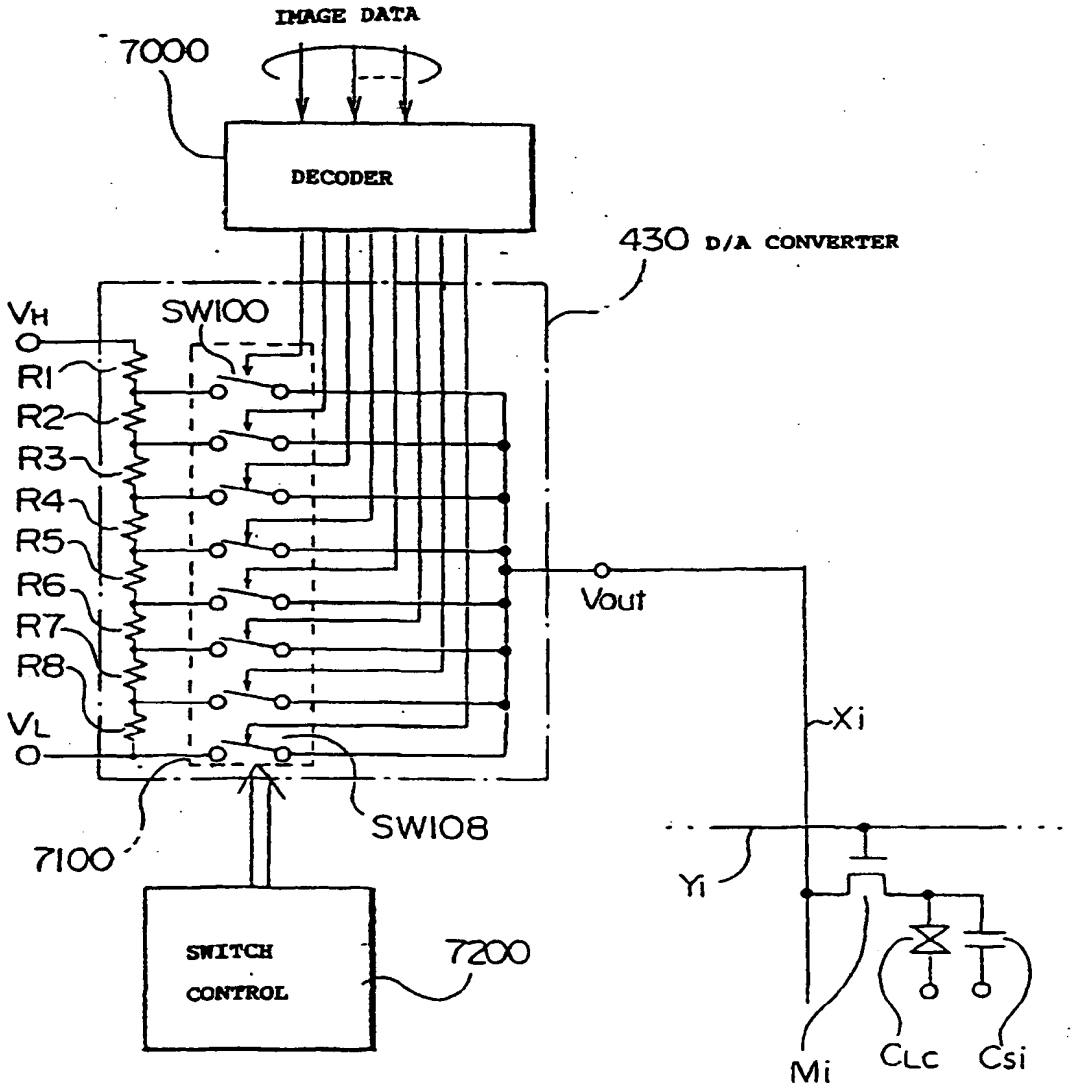


FIG. 14

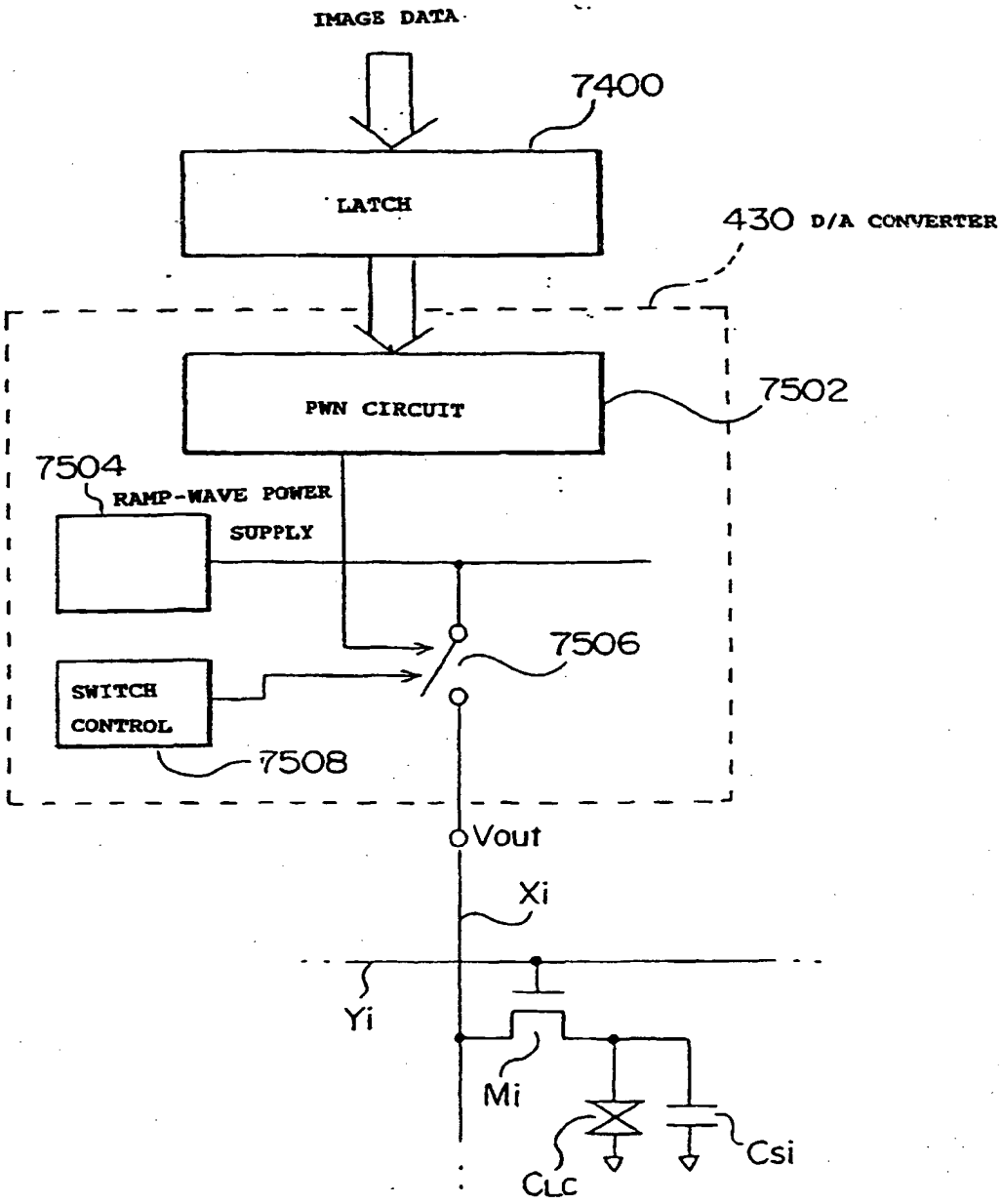


FIG. 15

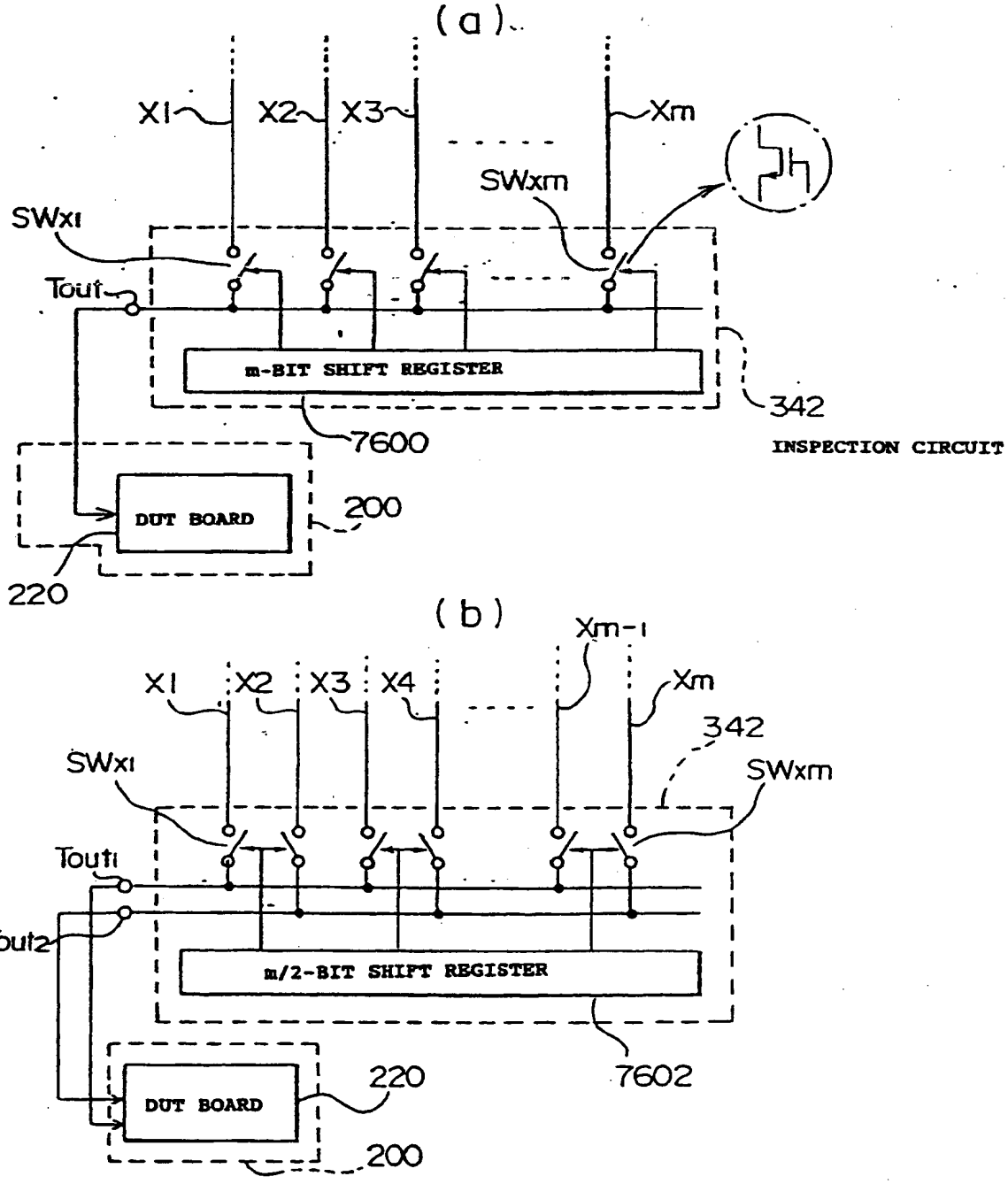


FIG. 16

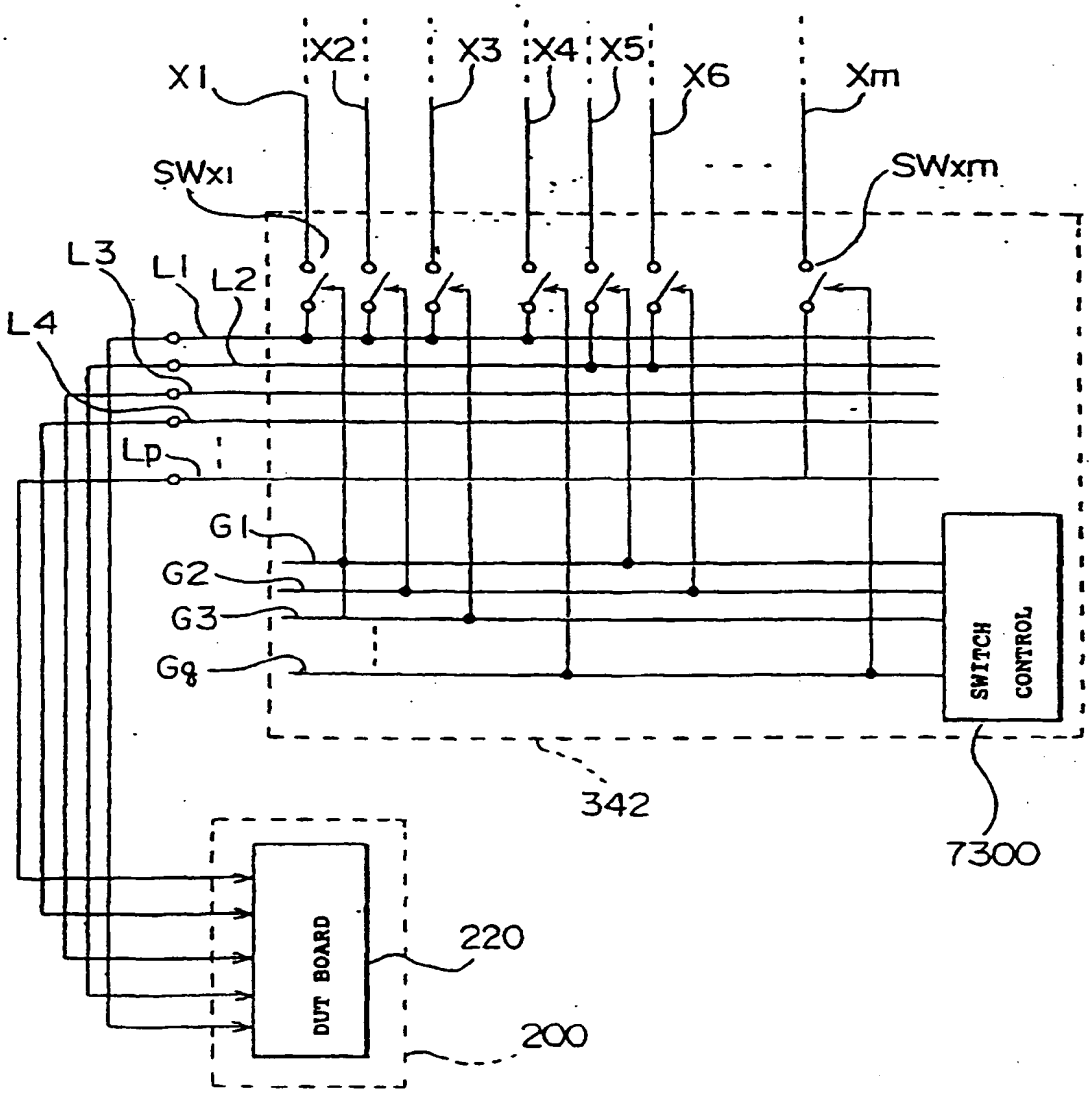


FIG. 17

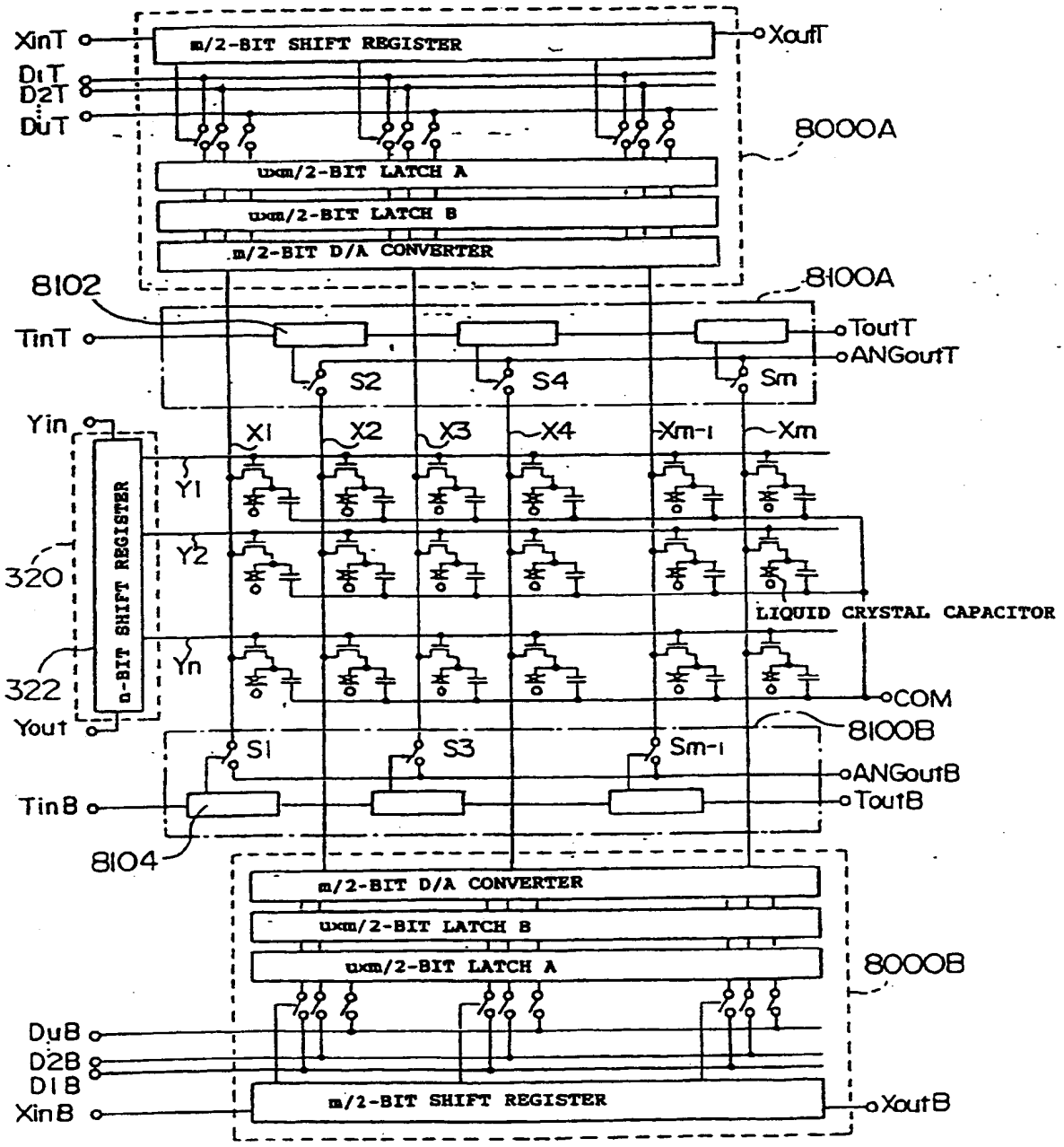


FIG. 18

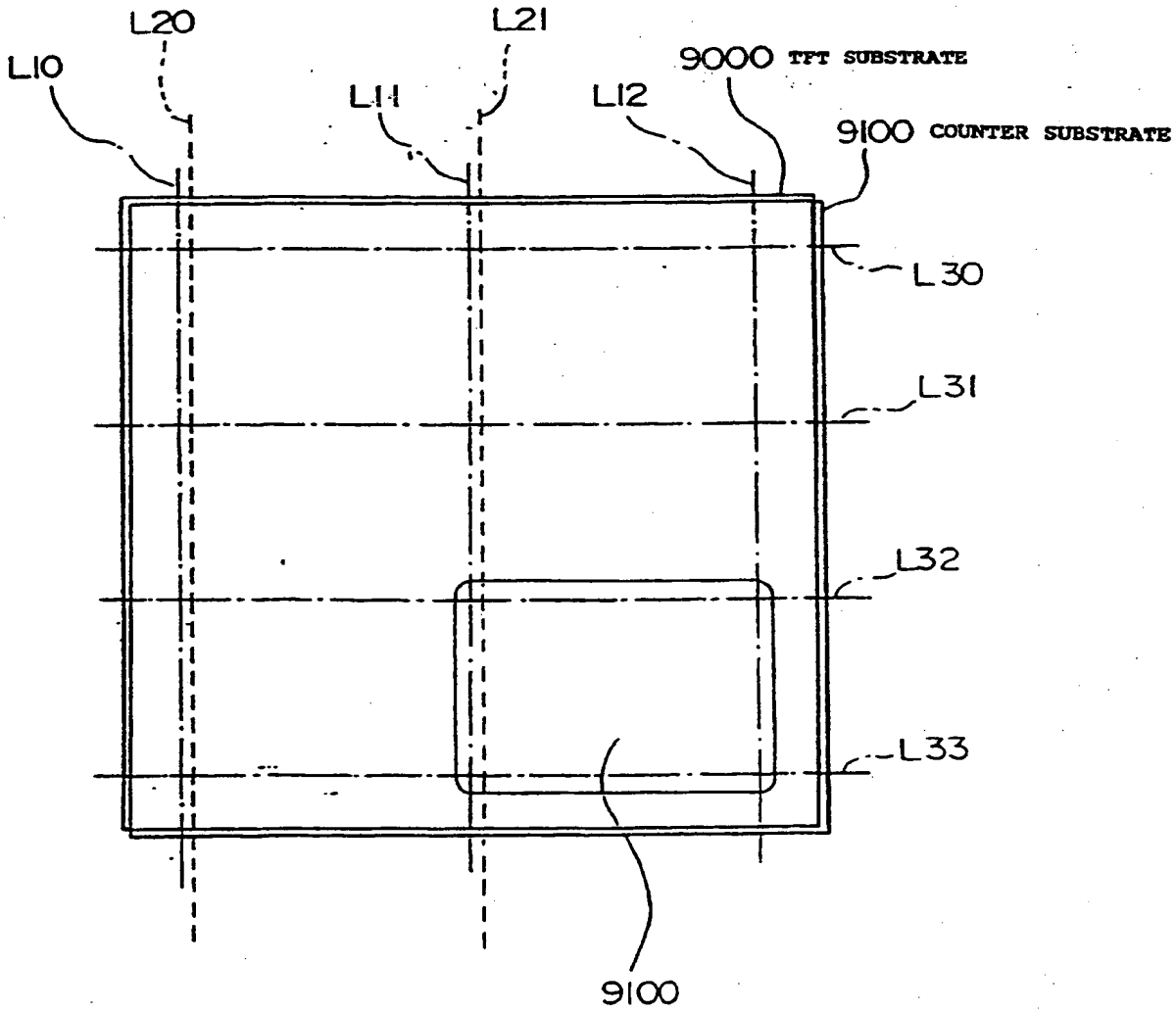


FIG. 19

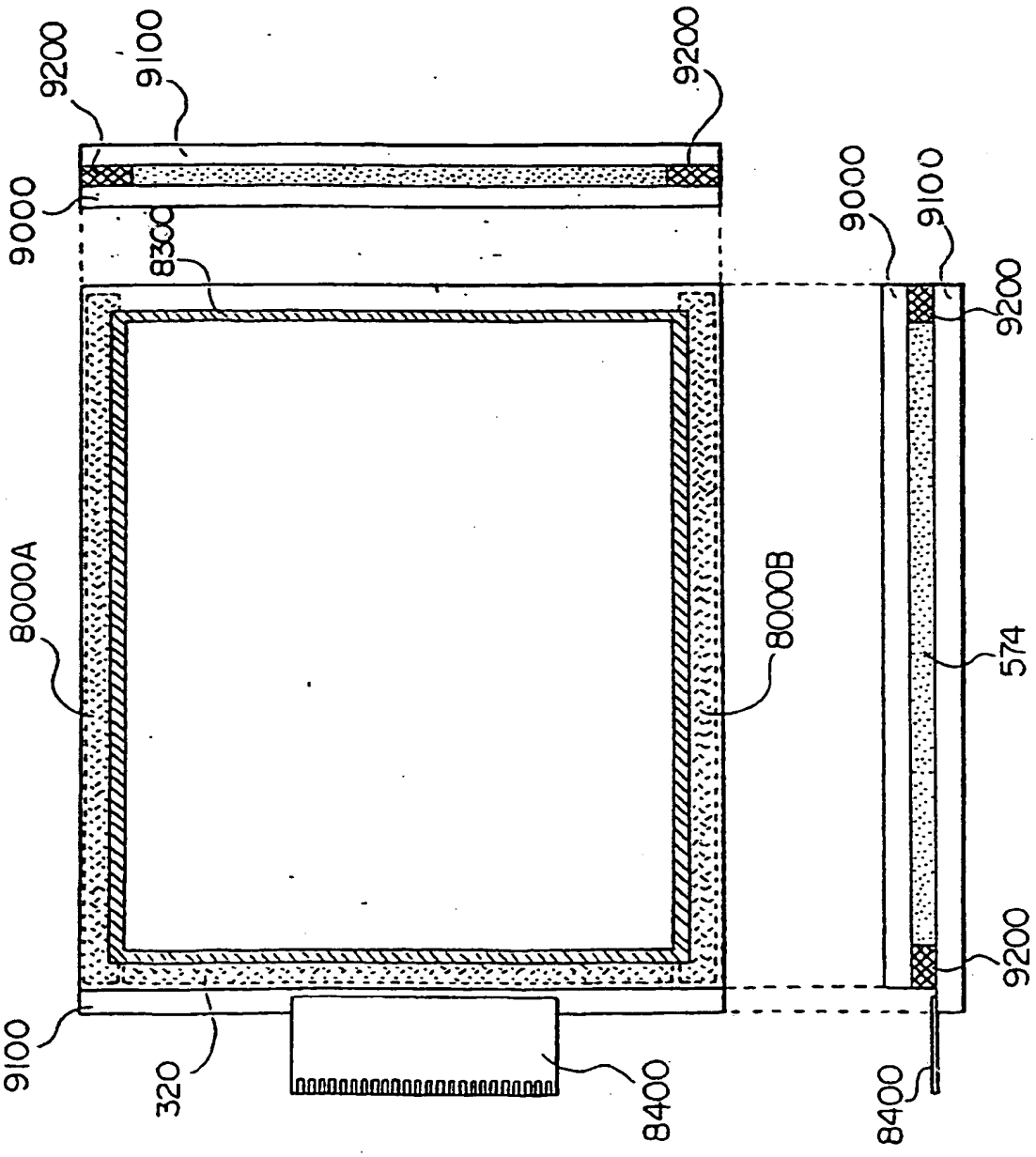


FIG. 20

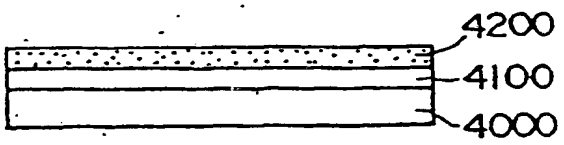


FIG. 21

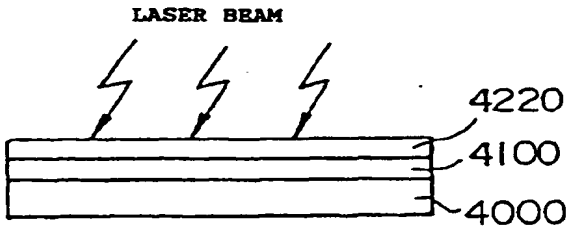


FIG. 22

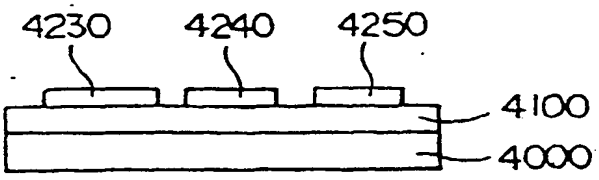


FIG. 23

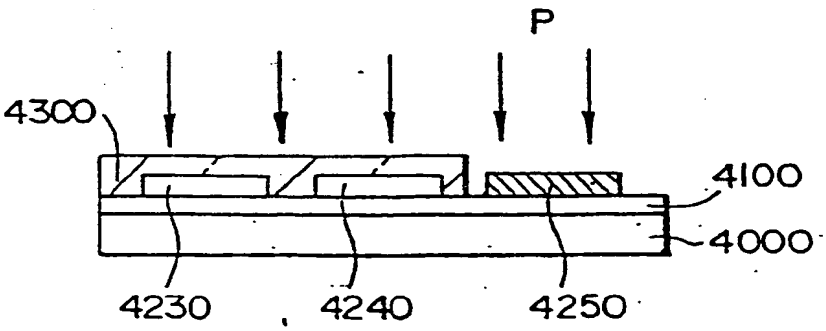


FIG. 24

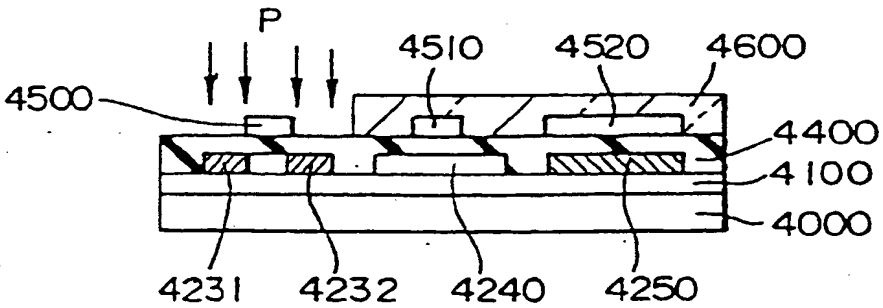
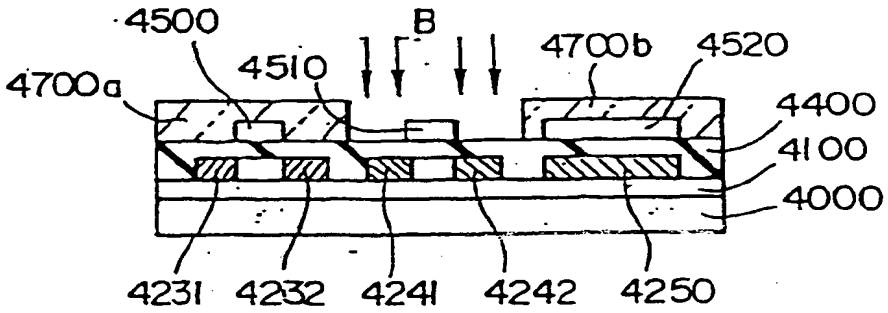


FIG. 25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4100
4000
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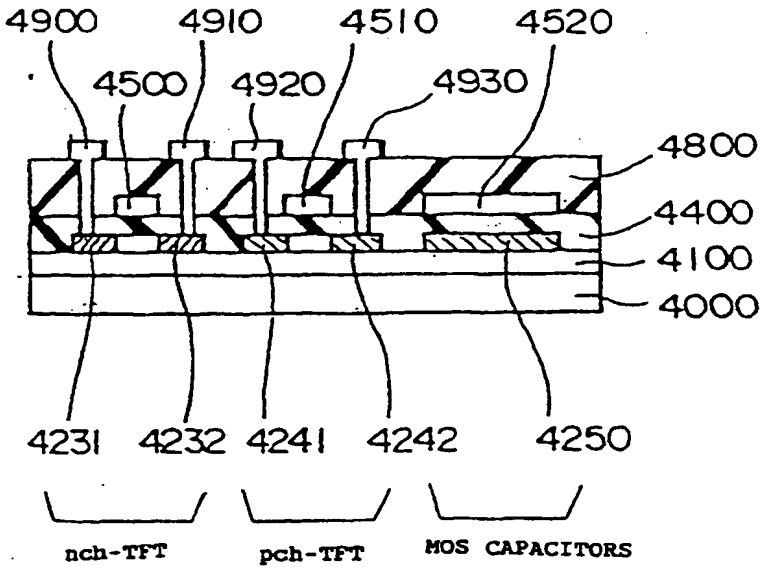
4232
4241
4242
4250

FIG. 26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4930
4800
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4232
4241
4242
4250
nch-TFT
pch-TFT
MOS CAPACITORS

FIG. 27

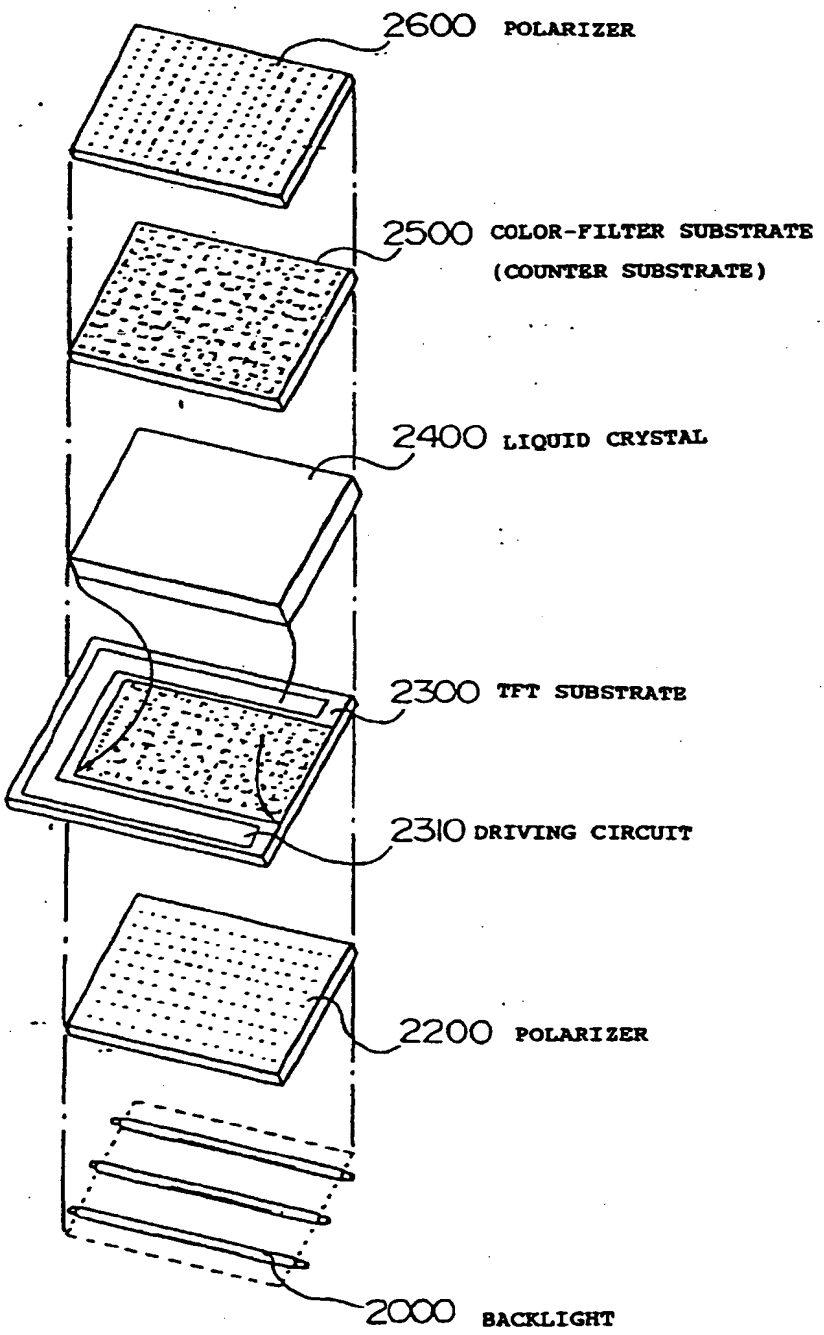


FIG. 28

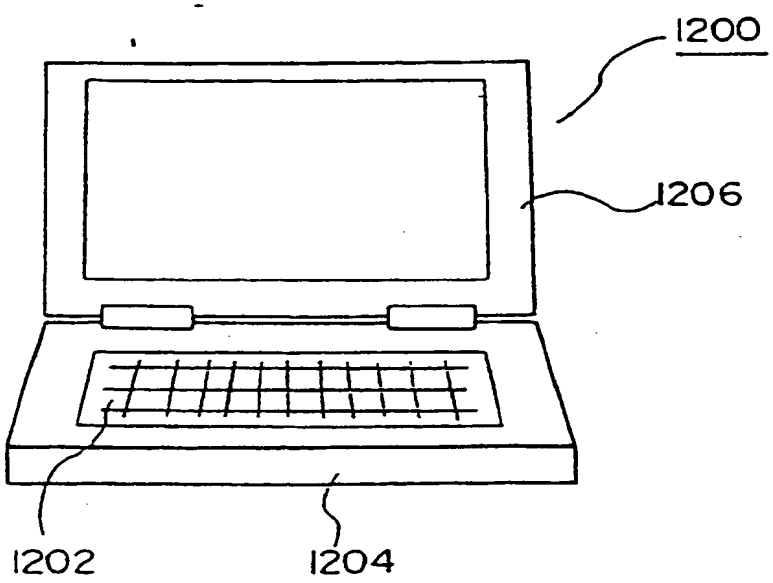


FIG. 29

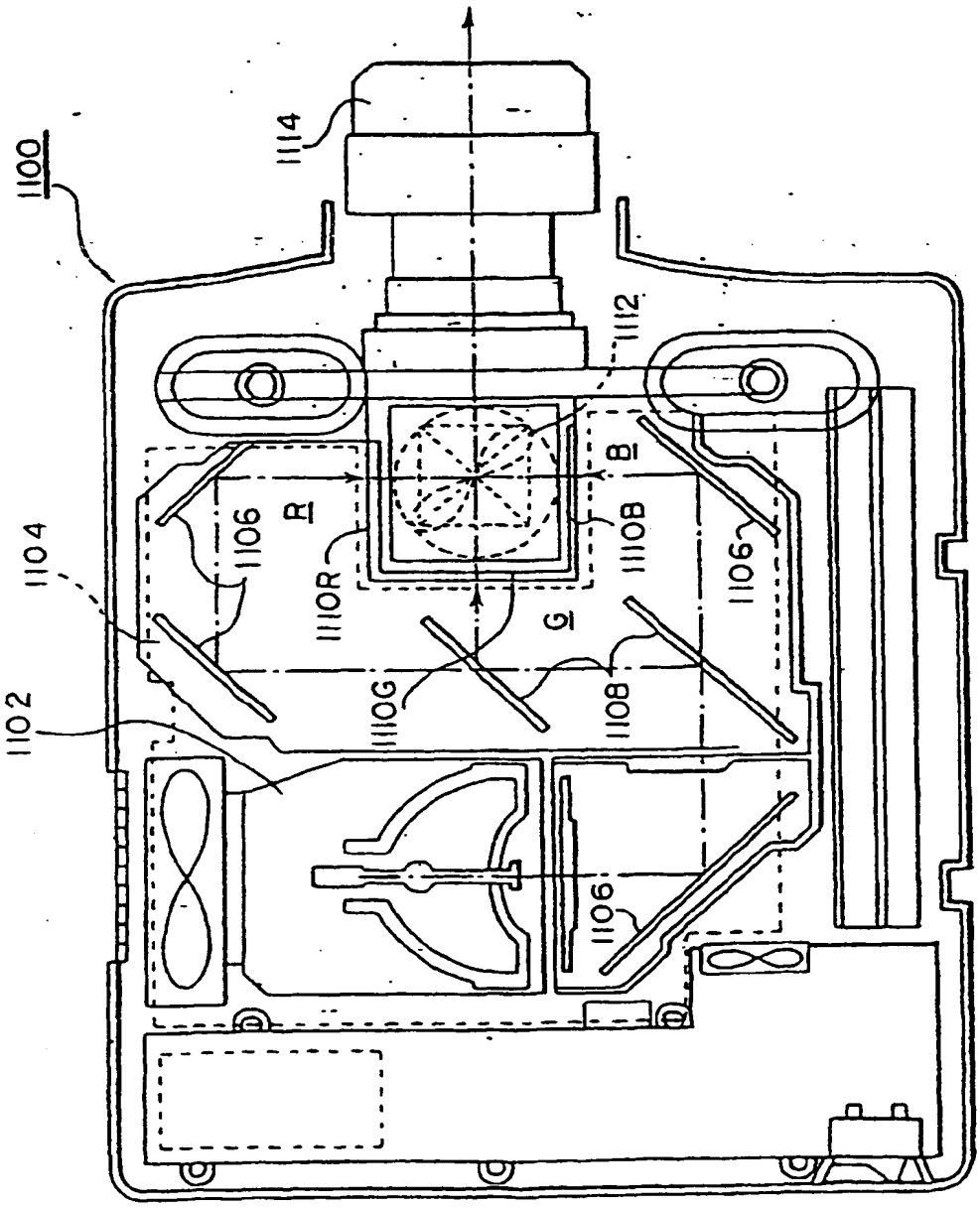
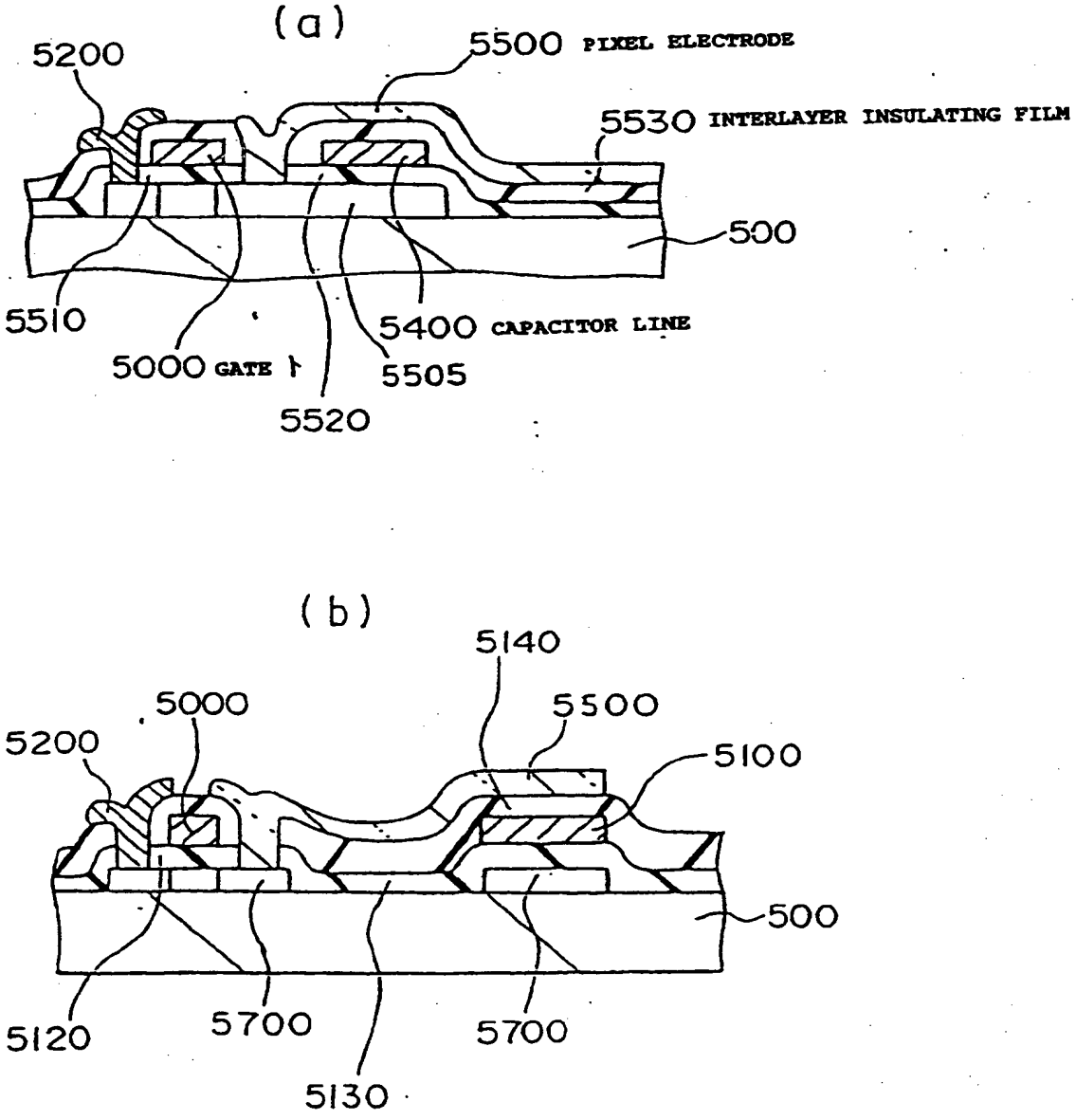


FIG. 30



INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP98/00405

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl[6] G09G3/36

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[6] G09G3/18, 3/36, G02F1/133

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Kokai Jitsuyo Shinan Koho 1926-1998 Toroku Jitsuyo Shinan Koho 1994-1998
Jitsuyo Shinan Koho 1971-1998

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP, 2-154292, A (Matsushita Electric Industrial Co., Ltd.), June 13, 1990 (13. 06. 90) (Family: none)	1-16
Y	JP, 5-94159, A (Matsushita Electric Industrial Co., Ltd.), April 16, 1993 (16. 04. 93) (Family: none)	1-16
Y	JP, 2-245794, A (Matsushita Electric Industrial Co., Ltd.), October 1, 1990 (01. 10. 90) (Family: none)	1-16
Y	JP, 63-52121, A (Seiko Instruments Inc.), March 5, 1988 (05. 03. 88) (Family: none)	6-16
Y	JP, 64-9375, A (Seiko Epson Corp.), January 12, 1989 (12. 01. 89) (Family: none)	11-14
Y	JP, 62-131233, A (Hitachi, Ltd.), June 13, 1987 (13. 06. 87) (Family: none)	13

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
April 6, 1998 (06. 04. 98)	April 21, 1998 (21. 04. 98)
Name and mailing address of the ISA/ Japanese Patent Office	Authorized officer
Facsimile No.	Telephone No.

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